DEC STD 176-0 Printed-Wiring Board Acceptance Criteria

DOCUMENT IDENTIFIER: A-DS-EL00176-00-0000 Rev M, 11-Nov-1992

ABSTRACT: This standard specifies criteria for rigid printed-wiring boards (PWBs) fabricated by or purchased for Digital Equipment Corporation.

APPLICABILITY: It is mandatory that PWBs fabricated by Digital manufacturing facilities or purchased from qualified suppliers meet or exceed all applicable specifications found in this standard unless modified by related Digital engineering drawings and specifications.

STATUS: APPROVED 11-Nov-1992; use VTX SMC for current status.

This document is confidential and proprietary, and is the property of Digital Equipment Corporation. This is an unpublished work protected under applicable copyright laws.

© Digital Equipment Corporation 1989, 1992. All rights reserved.

DEC STD 176-0 Printed-Wiring Board Acceptance Criteria

DOCUMENT IDENTIFIER: A-DS-EL00176-00-0000 Rev M, 11-Nov-1992

REVISION HISTORY:	Rev E,	18-Jun-1985	ECO Number APO04
	Rev F,	09-Dec-1986	ECO Number LJO05
	Rev H,	18-Dec-1987	ECO Number LJO06
	Rev J,	31-Jul-1989	ECO Number CTS07
	Rev K,	17-Jun-1991	ECO Number CTS08
	Rev L,	18-Nov-1991	ECO Number NRO09
	Rev M,	11-Nov-1992	ECO Number NRO10

Document Management Category:	Board Manufacture (MB)
Responsible Department:	Corporate Printed-Wiring Board Group
Responsible Person:	Gerald G. Gagnon
SMC Writer:	Eric Falkof

APPROVAL: This document has been reviewed and recommended for approval by the General Review group for its category and the Printed-Wiring Board DEC STD 176 Advisory Committee.

Gerald G. Gagnon - Corporate Printed-Wiring Board Group

Eric Williams - Standards Process Manager

Direct requests for further information to:

Gerald G. Gagnon
Use $ VTX ELF for the latest location information.

Use VTX SMC to order copies of this document from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

The DIGITAL logo and VAXBI are registered trademarks of Digital Equipment Corporation.
UL is a registered trademark of Underwriters Laboratories
VALU is a trademark of E.I. duPont de Nemours and Co.

CONTENTS

1 INTRODUCTION 1
1.1 SCOPE 1
1.2 RESPONSIBILITIES 1
1.2.1 Digital Organizations 1
1.2.2 Suppliers 1
1.2.3 PWB Standards Committee 1

2 GENERAL REQUIREMENTS 1
2.1 TERMINOLOGY 1
2.2 COMPOSITION AND PROCESSING 1
2.3 OVERALL CONFIGURATION AND CONSTRUCTION 1
2.4 MICROSECTIONING AND MAGNIFICATION 2
2.5 NUMERIC ROUNDING CONVENTION 2
2.6 FABRICATION MATERIALS 2
2.6.1 Copper-Clad Laminates 3
2.6.2 Prepreg 3
2.6.3 Copper Foil 3
2.6.4 Soldermask 4
2.6.5 Plating Materials 4
2.7 WORKMANSHIP AND CLEANLINESS 5
2.8 IDENTIFICATION MARKINGS 5
2.9 COLORS 8
2.10 DIMENSIONS AND TOLERANCES 8

3 OUTSIDE CONFIGURATION 9
3.1 LENGTH AND WIDTH 9
3.2 THICKNESS—FINGERLESS BOARDS 9
3.3 THICKNESS—PWBS WITH FINGERS 10
3.4 WARPAGE 11
3.5 SLOTS, NOTCHES, AND CUTOUTS 11
3.6 STRAIGHTNESS, PARALLELISM, AND SQUARENESS 11

4 BASE MATERIAL VISUAL CHARACTERISTICS 12
4.1 SURFACE AND SUBSURFACE CONDITIONS 12
4.2 CHIPS, CRACKS, FIBERS, AND HALOING—LAMINATE 12
4.3 DELAMINATION, CRAZING, AND MEASLING 12

5 HOLES 14
5.1 NONPLATED DRILLED AND PUNCHED HOLES 14
5.1.1 Nonplated Hole Diameters 14
5.1.2 Chips, Cracks, Delamination, Fibers, Haloing— Drilled and Punched Holes . . . 14
5.1.3 Missing and Extra Holes 14
5.2 PLATED-THROUGH HOLES (PTH) 15
5.2.1 Plated-Hole Diameters 15
5.2.2 Plating Thicknesses 16
5.2.3 Other PTH Characteristics 17

5.3 HOLE LOCATION ACCURACY (HLA) 23

6 CONDUCTORS AND PADS 24
6.1 CONDUCTOR WIDTHS (INNER AND OUTER LAYER) 24
6.1.1 Thermal Impedance Conductors (Legs) 24
6.2 SPACING (INNER AND OUTER LAYER) 24
6.3 PAD DIAMETERS (INNER AND OUTER LAYER) 25
6.4 ANNULAR RINGS—MAXIMUM ALLOWABLE MISREGISTRATION FOR MSL AND NON-MSL TECHNOLOGIES 26
6.4.1 Inner Layer and Outer-Layer Features 26
6.4.2 Power and Ground Planes or Thermal Impedance Pad Areas 29
6.5 PLATING THICKNESSES—ETCH LINES 30
6.6 ETCH CHARACTERISTICS 31
6.7 OTHER ETCH CHARACTERISTICS 31

7 PLATING CHARACTERISTICS 33
7.1 TIN-LEAD PLATING (FUSED) 33
7.2 ADHESION 33
7.3 BOND STRENGTH (TERMINAL PULL STRENGTH) 33
7.4 SOLDERABILITY 33
7.5 THERMAL STRESS (PLATED-THROUGH HOLES) 33

8 FINGERS 34
8.1 PLATING THICKNESSES 34
8.2 SURFACE FINISH 34
8.3 POROSITY 34
8.4 UNUSED FINGERS 35
8.5 ADHESION 35
8.6 LENGTH 35
8.7 WIDTH 35
8.8 SPACING 35
8.9 BEVEL 36
8.10 HEXBOARD EDGE TAPER 36
8.11 OTHER FINGER CHARACTERISTICS 37
8.11.1 Breaks, Flaking, Peeling, and Wrinkling 37
8.11.2 Discoloration 37
8.11.3 Dents, Inclusions, Nicks, Nodules, Pinholes, Pits, Scratches, and Voids 37

9 SOLDERMASK 41
9.1 TYPES 41
9.2 PLACEMENT 41
9.2.1 Board Side 41
9.2.2 Spacing/Coverage/Thickness Requirements 41
9.3 CURE 43
9.4 SOLVENT AND FLUX RESISTANCE 43
9.5 FLAMMABILITY 43
9.6 ABRASION RESISTANCE 44
9.7 ADHESION 44
9.8 SOLDER RESISTANCE 44

9.9 OTHER SOLDERMASK CHARACTERISTICS 44
9.9.1 Blistering 44
9.9.2 Voids 45
9.9.3 Exposed Conductors and Pads 45
9.9.4 Exposed Copper 45
9.9.5 Placement Defects 45

10 MULTILAYER (ML) AND MULTISIGNAL-LAYER (MSL) PWBs 46

11 AUTOTHIEVING AND OTHER NONCONDUCTOR ETCH 47
11.1 AUTOTHIEVING 47
11.2 NONCONDUCTOR ETCH 47

12 BACKPANEL BOARDS 47
12.1 BACKPLANE CONNECTOR HOLE SIZES 47
12.1.1 Press-Pin Backplane Primary Hole Size 48
12.1.2 Press-Pin Backplane Finished Hole Size 48
12.1.3 Wave Solder Backplane Hole Sizes 48
12.1.4 Other Backplane Hole Sizes 48
12.2 UNIQUE BACKPLANE REQUIREMENTS 48
12.2.1 Backplanes with Solder Connector Contact Pads 48

13 ELECTRICAL CHARACTERISTICS 51
13.1 CONDUCTOR INTERCONNECTION RESISTANCE 51
13.2 CONTINUITY 51
13.3 ADDITIONAL ML AND MSL REQUIREMENTS 51
13.3.1 Dielectric Withstanding Voltage (HIPOT) 51
13.3.2 Insulation Resistance 52
13.3.3 Current Capacity 52
13.3.4 Impedance 52
13.3.5 Capacitance 52
13.3.6 Thermal Stress—ML and MSL PWBs 53

14 ALLOWABLE REPAIRS 54

15 PRODUCT SAFETY 54

16 PACKAGING 54

17 QUALITY ASSURANCE TESTS 55

Appendix A POROSITY PROCEDURE 57

A.1 CONTACT POROSITY 57
A.1.1 EQUIPMENT 57
A.1.2 REQUIREMENT 58

A.1.3 METHOD 58
A.1.3.1 Cleaning and Handling Specimens 58
A.1.3.2 Equipment Preparation 58
A.1.3.3 Nitric Acid Vapor Test 59
A.1.3.4 Corrosion Product Examination 59
A.1.3.5 Corrosion Product Report and Evaluation Data Requirements 60
A.1.4 DATA INTERPRETATION 60

Appendix B CALCULATION AND CONVERSION OF TRUE POSITION TOLERANCE 61

B.1 TO CONVERT GEOMETRIC LOCATION (±) TOLERANCE (GLT) TO TRUE POSITION DIAMETER (TPD): 61

B.2 TO CONVERT FROM TRUE POSITION DIAMETER TO GEOMETRIC LOCATION (±) TOLERANCE: 61

Appendix C WARPAGE MEASUREMENT PROCEDURE 63

C.1 SCOPE 63

C.2 APPLICABILITY 63

C.3 DEFINITIONS 63
C.3.1 BOW 63
C.3.2 TWIST 63
C.3.3 BOW AND TWIST 63

C.4 LIMITATIONS AND PRECAUTIONS 64

C.5 APPARATUS 64

C.6 PROCEDURES 64
C.6.1 BOW 64
C.6.2 TWIST 66
C.6.2.1 TWIST AXIS ON THE DIAGONAL 66
C.6.2.2 TWIST AXIS NOT ON THE DIAGONAL 69
C.6.3 BOW AND TWIST 70

Appendix D THERMAL STRESS TEST PROCEDURE 71

D.1 SCOPE 71

D.2 TEST SPECIMENS 71
D.2.1 SPECIMEN TYPE 71
D.2.2 SPECIMEN LOCATION 71
D.2.3 SPECIMEN DIMENSIONS/REMOVAL 71
D.2.4 QUANTITY OF TEST SPECIMENS 72

D.3 APPARATUS 72
D.3.1 BAKE OVEN 72
D.3.2 SOLDER POT 72

D.3.3 SOLDER 73
D.3.4 TEMPERATURE INDICATOR 73
D.3.5 FLUX 73
D.4 PROCEDURE 73
D.4.1 OVEN CONDITIONING 73
D.4.2 FLUXING 73
D.4.3 SOLDER FLOAT 73
D.4.4 SPECIMEN COOL DOWN 73
D.4.5 SPECIMEN PREPARATION FOR METALLOGRAPHIC ANALYSIS 74
D.4.6 MICROSECTION PREPARATION 74
D.4.7 MICROSECTION ANALYSIS 74

Appendix E METRIC HOLE SIZE SELECTIONS CORRESPONDING TO DIGITAL STANDARD U.S. CUSTOMARY REQUIREMENTS 75

Appendix F PRINTED-WIRING BOARD CONFIGURATIONS 77
F.1 CONFIGURATIONS 77

Appendix G REFERENCED DOCUMENTS 79
G.1 Digital Documents, EL-Class 79
G.2 Documents External to Digital 79
G.3 Digital Drawings 79
G.4 Digital Purchase Specifications 80
G.5 Federal and Military Publications 81
G.6 IPC (Institute of Printed Circuits) Publications 81
G.7 Other Publications 82

Appendix H RELATED DOCUMENTS 83
H.1 Digital Purchase Specifications 83
H.2 Federal and Military Publications 83
H.3 IPC (Institute of Printed Circuits) Publications 83
H.4 Other Publications 84

INDEX

FIGURES

1	Typical Printed-Wiring Board Manufacturing Panel Layout	7
2	Measling, Crazing, and Delamination	13
3	Barrel and Pad	16
4	Plating Thickness and Quality	17
5	Plated-Through Hole Evaluated in *As Received* Condition	20
6	Plated-Through Hole Evaluated After Thermal Stress	20
7	Typical Power/Ground Plane Thermal Impedance Pad	24
8	Preferred Hole-to-Pad Registration	26
9	Maximum Hole-to-Pad Breakout	27
10	Minimum Clearance Between Hole and Conductor-Pad Interface —Without Elongated Pad	28
11	Preferred Hole-to-Pad Registration—Thermal Impedance Pads	29
12	Maximum Allowable Breakout of Hole-to-Thermal Impedance Pad	29
13	Minimum PTH-to-Inner Layer Plane Clearance	30
14	Plating Thickness—Etch Lines	30
15	Etch Undercutting	31
16	Etch Imperfections	32
17	Bevel—Finger Edge	36
18	Edge Taper	36
19	Minimum Gold-Plating Length (Dimension A) and Critical Contact Area (Dimension B)	40
20	Soldermask Foot-to-Base Laminate	42
21	Solder Backplane Critical Contact Area	50
22	Position Tolerance	61
23	Bow (Top View)	65
24	Bow (Side View)	65
25	Twist—Natural Resting Position (Concave) Without Added Force	67
26	Twist—Natural Resting Position (Convex) Without Added Force	68
27	Twist—(Concave)	69

TABLES

1	Magnification	2
2	Copper Foil Thicknesses	10
3	Maximum Warpage	11
4	Maximum Allowable Extensions—Laminate	12
5	Nonplated Hole Diameters	14
6	Maximum Allowable Extensions—Drilled/Punched Holes	14
7	PTH Diameters and Tolerances*	15
8	Conductor Widths	24
9	Spacing	25
10	Pad Diameters	25
11	Plating Thickness—Etch Lines	30
12	Copper Foil Thicknesses	46
13	Defect Criteria—F and T Backplane Connector Solder Pads	50
14	IPC-TM-650 Quality Assurance Tests	55

15 Metric Hole Size Selections 75
16 Printed-Wiring Board Configuration 77

1 INTRODUCTION

This standard specifies criteria for rigid printed-wiring boards (PWBs) fabricated by or purchased for Digital Equipment Corporation.

1.1 SCOPE

This standard specifies the finished product acceptance criteria for rigid PWBs designed to meet Digital standard design requirements unless modified by Digital engineering drawings and specifications. This standard applies to all PWB types and technologies. This standard does not apply to flexible circuits or ceramic printed-wiring substrates.

1.2 RESPONSIBILITIES

1.2.1 Digital Organizations

All internal organizations involved in the fabrication, procurement, and use of PWBs are responsible for understanding and complying to the requirements in this document and for providing information to keep the document up-to-date.

1.2.2 Suppliers

Suppliers under contract to produce PWBs for Digital must comply with the requirements of this standard.

1.2.3 PWB Standards Committee

Refer to EL-SM176-00, *Printed-Wiring Board Manual*, for a list of committee members.

2 GENERAL REQUIREMENTS

Whether fabricated in Digital manufacturing facilities or purchased from qualified suppliers, all PWBs shall meet or exceed all applicable specifications found in this standard, as modified only by related Digital drawings and specifications.

2.1 TERMINOLOGY

The definitions of all printed-wiring terms used in this standard shall be as specified in *DEC STD 016-0 Printed-Wiring Board and Module Manufacturing Terminology.*

2.2 COMPOSITION AND PROCESSING

The composition and processing of the types of PWBs covered by this standard shall be as described in DEC STD 016-0.

2.3 OVERALL CONFIGURATION AND CONSTRUCTION

The conductive and nonconductive patterns, including fingers, plated-through holes and associated hole pads (PTH), and the overall configuration of each board, including slots, notches, and cutouts, shall be as specified in the master drawing and as delineated in the artwork master. See Appendix E, Referenced Documents, for applicable drawings.

Unless specified otherwise, all PWBs and backplanes must be capable of complying with reliability tests (such as thermal stress) specified in this document.

2.4 MICROSECTIONING AND MAGNIFICATION

Microsection inspections shall be in accordance with text under subhead 2.1.1 of IPC-TM-650, *Test Methods Manual*.

The appropriate magnification for defect detection is specified in Table 1. When a defect is suspected at these magnifications, higher magnification may be used to verify conformance and/or assist in determining the root cause. Defects found at higher magnification are considered defects.

Table 1: Magnification

Item(s) Inspected	Minimum Magnification (X)
Overall cosmetic quality	Visual
Board features	2
Referee inspection of board features	10
Plating quality in microsections	200
Plating and soldermask thickness in microsections	400

2.5 NUMERIC ROUNDING CONVENTION

When numeric measurements are made to greater precision than is required by this standard, it becomes necessary to round results to a specified value in order to determine conformance. The following rounding convention shall be used:

- The figure in the last place to be retained shall be kept unchanged when the figure in the next place is less than 5.
- The figure in the last place to be retained shall be increased by 1 when the figure in the next place is greater than or equal to 5.
- The final figure shall be obtained from the most precise value available and not from a series of successive roundings.

2.6 FABRICATION MATERIALS

Fabrication materials are specified below for informational purposes only. Such materials include copper-clad laminates, prepreg, copper foil, soldermask, and plating materials.

2.6.1 Copper-Clad Laminates

All copper-clad laminates shall meet the requirements of the latest revisions of Digital purchase specifications:

A-PS-1400000-GS	*Basic Specification for Printed-Wiring Board Materials*
A-PS-1400001-GS	*Glass Epoxy Panels (No Copper)*
A-PS-1400002-GS	*Micarta Panels (Blue and Black)*
A-PS-1400008-GS	*Copper-Clad Thin Laminates (Raw Stock 0.031 Inch Thick or Less)*
A-PS-1400011-GS	*Copper-Clad Thick Laminates (Raw Stock >0.031 Inch Thick)*
A-PS-1400016-GS	*Mass Molded Laminates*
A-PS-1400018-GS	*Copper-Clad Thin Laminates for Multisignal Layer PWBs*
A-PS-1400023-GS	*Polyimide Copper-Clad Laminates for ML PWBs*
A-PS-1400025-GS	*Copper Clad Laminates Utilizing Planar Resistor Foils*
A-PS-1400026-GS	*CEM-3 Copper-Clad Thick Laminates (Raw Stock >0.031 Inch)*
A-PS-1400027-GS	*Laminates, Copper-Clad for Multilayer PWBs Utilizing Bismalemide-triazine*

All laminates must be recognized by Underwriters Laboratories (UL). Refer to *DEC STD 176-2 Printed-Wiring Board Product Safety Criteria* for the UL recognition requirements.

All laminates must be listed on the Digital Qualified Vendor List (QVL). Internal sources of supply should contact James Apruzzi for the QVL listing; see VTX ELF for location information. External sources of supply should contact the appropriate Digital purchasing agent.

2.6.2 Prepreg

Resin preimpregnated B-stage (semicured) continuous-filament fiber glass cloth sheets shall meet the requirements of the latest revision of Digital purchase specifications:

A-PS-1400000-GS	*Basic Specification for Printed-Wiring Board Materials*
A-PS-1400009-GS	*Preimpregnated Glass Cloth (B-stage)*
A-PS-1400017-GS	*Preimpregnated Glass Cloth for Multisignal Layer PWBs*
A-PS-1400024-GS	*Polyimide Preimpregnated Glass Cloth (B-stage) for ML PWBs*
A-PS-1400028-GS	*Bismalemide-triazine Preimpregnated Glass Cloth (B-stage) for Multilayer PWBs*

All prepregs must be UL recognized. Refer to DEC STD 176-2 for the UL recognition requirements. Internal sources of supply should contact James Apruzzi for the QVL listing; see VTX ELF for location information. External sources of supply should contact the appropriate Digital purchasing agent.

2.6.3 Copper Foil

The copper foil used in the fabrication of laminates and printed-wiring boards shall be in accordance with the latest revisions of Digital purchase specifications:

A-PS-1400000-GS	*Basic Specification for Printed-Wiring Board Materials*
A-PS-1400015-GS	*Copper Foil for PWBs—Sheets and Rolls*

Copper foil must be listed on the Digital Qualified Vendor List (QVL). Internal sources of supply should contact James Apruzzi for the QVL listing; see VTX ELF for location information. External sources of supply should contact the appropriate Digital purchasing agent.

2.6.4 Soldermask

The soldermask shall be a permanent polymer coating or photopolymer film that will prevent solder bridging during component assembly operations. Soldermask shall:

a. Conform to the Class II requirements of the latest revision of IPC-SM-840, *Qualification and Performance of Permanent Polymer Coating (Soldermask) for Printed Boards.*

b. Be UL recognized. Refer to DEC STD 176-2.

c. Conform to the requirements of the text of subhead 9.

d. Conform to EL-MF543-00, *Procedure for Soldermask Evaluation*.

e. Be listed on the Digital Qualified Vendor List (QVL). Internal sources of supply should contact Richard Barnett for the QVL listing; see VTX ELF for location information. External sources of supply should contact the appropriate Digital purchasing agent.

All soldermask shall be in accordance with the latest revisions of Digital purchasing specifications:

A-PS-1400029-GS	*Soldermask—Photoimageable Liquid or Screened Liquid*
A-PS-1400030-GS	*Soldermask—Photosensitive Dry Film*
A-PS-1400031-GS	*Copper Chelating Material (Coating) All Copper*

2.6.5 Plating Materials

The plating materials specified below, or approved functional equivalents, are acceptable for Digital PWBs. Plating thicknesses are specified under subheads 6.5 and 8.1.

a. Electroless copper—A suitable electroless (chemical) copper deposition material adherent to plastic and copper must be utilized in a preliminary process that provides a conductive layer over nonconductive base materials prior to the electroplating of PTHs.

b. Electrolytic copper—All electrolytically deposited copper plating shall conform to MIL-C-14550, *Copper Plating, Electrodeposited*, Class 1, and have a minimum purity of 99.5 percent as determined by ASTM E53-48, *Standard Method for Chemical Analysis of Copper (Electrolytic Determination).*

c. Electrolytic tin-lead—Tin-lead alloy electroplating shall conform to MIL-P-81728, *Plating, Tin-lead, Electrodeposited* and be composed of 60 ± 10 percent tin and 40 ± 10 percent lead by volume.

d. Electrolytic nickel—All electrolytically deposited nickel plating shall be low stress and conform to QQ-N-290, *Nickel Plating, Electrodeposited,* Class 2.

e. Electrolytic gold—Gold electroplating shall conform to MIL-G-45204, *Gold Plating, Electrodeposited*, Type II, Grade C. It must also be uniform in quality and have a purity of at least 99 percent.

2.7 WORKMANSHIP AND CLEANLINESS

When tested after proper removal from shipment packaging, there shall be no contaminations or imperfections that affect form, fit, function, reliability, serviceability, or processability within a module application.

PWB ionic (electrical) contaminants measured according to Digital engineering specification EL-MF299-00, *Printed Circuit Boards/Modules: Cleaning Process Contamination* shall not exceed 10 mg/sq. in (NaCl equivalent).

2.8 IDENTIFICATION MARKINGS

All *on-circuit* markings specified and placed in the PWB design data base, according to Digital standard design requirements, shall appear on each circuit.

Certain markings for designs produced to earlier revisions of Digital design standards may be subject to the *grandfathering* clause stated within those standards. However, every effort should be made to consult Producibility (internal suppliers) and Digital Purchasing (external suppliers) to ensure that markings are consistent with current requirements.

Regardless of the circumstances, the absolute minimum markings that must appear on each circuit (refer to Figure 1) in etch (or nonconductive permanent ink where applicable) are as follows.

a. PWB 50-class part number and revision, for example, 50-12345-01;B1.

b. Side 1 identification per design data.

c. Product safety (UL) required markings. (Refer to DEC STD 176-2.)

d. Traceability: The finished printed circuit board shall be marked in such a manner that it is traceable to the processes used to manufacture that board and to the raw materials (that is, prepregs, laminate, and copper) manufacturer, and manufacturing processes. This may be accomplished using the associated work order (traveler) for documentation.

e. Date of manufacture in Julian date code format (DDDYY) with one of the following time frames:

    1. Date of etching
    2. Date of soldermask
    3. Final inspection date
    4. Shipping date

f. HIPOT test stamp, if applicable. See text under subhead 13.3.1.

g. Unless specified otherwise, an electrical test stamp is required on each assembly board (see Figure 1). Where the assembly board contains more than one circuit, one test stamp may be applied to that assembly board providing:

    1. There is documented evidence (such as board electrical test program or test data sheet/log) that all circuits on the assembly board are tested to requirements in text under subhead 13.
    2. All circuits on the assembly board that fail electrical test and are scrapped are clearly identified (for example, punched out or crossed out) on side 1 and side 2.

h. The serialization markings and test data that required are described under the text in subhead 13.3.4, Impedance, and 13.3.5, Capacitance, shall serve as sufficient evidence that impedance/capacitance testing was performed at the supplier's site. No additional mark or stamp is required.

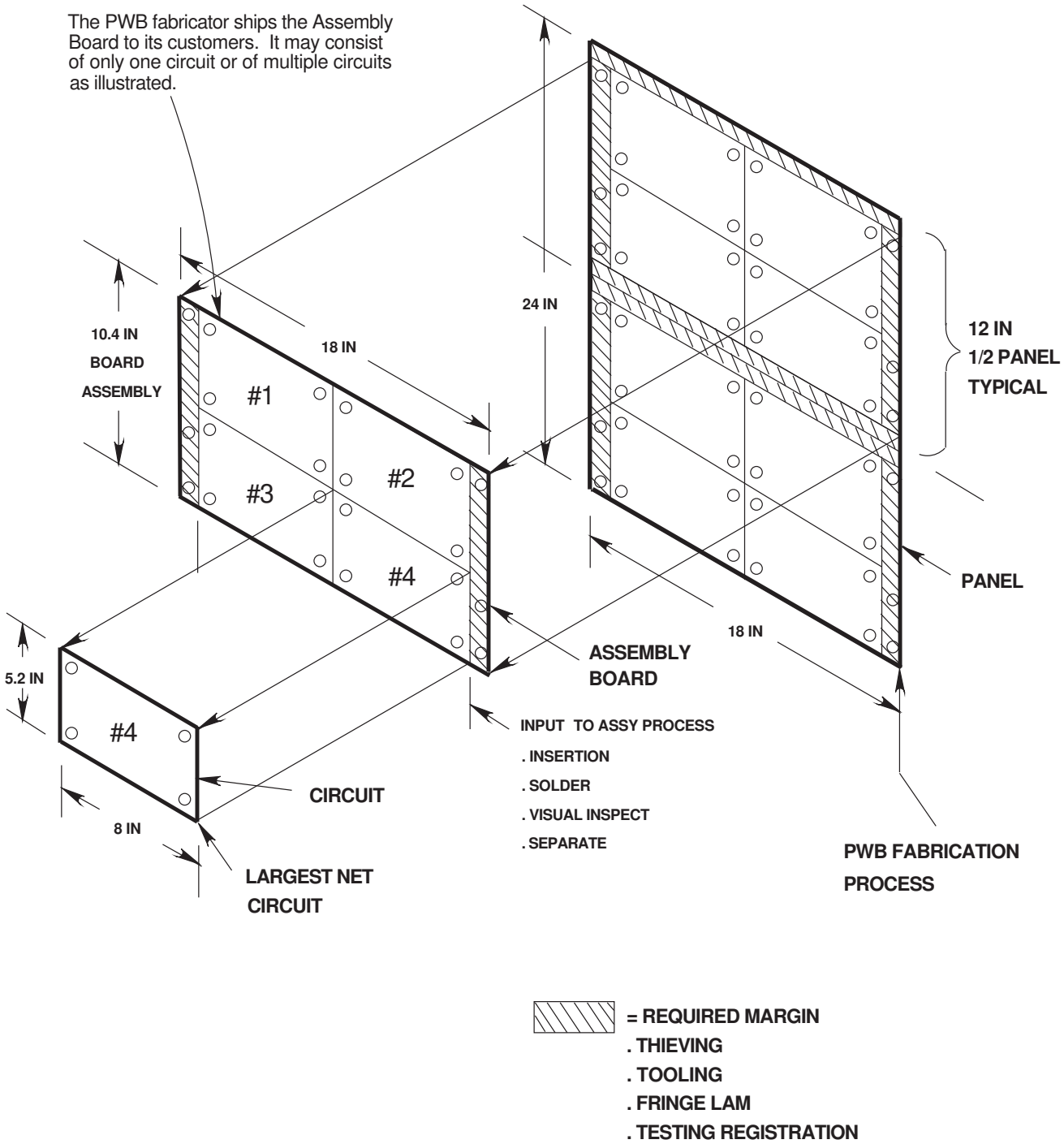
i. Unless specified otherwise, Quality Control (QC) lot acceptance stamp is required on each assembly board (see Figure 1). Where the assembly board contains more than one circuit, one stamp may be applied to that assembly board providing:

   1. There is documented evidence (such as QC inspection data sheets/logs, and so on) that all circuits on the assembly board were inspected.
   2. All circuits on the assembly board that fail inspection and are scrapped, are clearly identified (for example, punched out or crossed out) on side 1 and 2.

j. In addition, all markings shall meet the following criteria.

   1. Markings shall have no measurable effect on electrical or mechanical performance of the PWB.
   2. Markings shall be permanent and legible after the performance of all tests specified in this standard.
   3. Markings shall be compatible with all PWB materials and components.
   4. Markings shall be permanent and legible after module assembly process.

Figure 1: Typical Printed-Wiring Board Manufacturing Panel Layout



NOTE

This figure is intended to illustrate the relationship between panel-assembly-board-circuit using an 18 × 24 inch panel as an example. Other panel sizes may be produced but the panel-assembly-board-circuit relationship is still the same as illustrated.

2.9 COLORS

All PWBs shall be fabricated in the natural resin color supplied by the laminate manufacturer. Regardless of the colors used, the PWB manufacturer's name or trademark and the Digital part identifier (part number and revision) must be legible.

2.10 DIMENSIONS AND TOLERANCES

All dimensions and tolerances specified in this standard are applicable only to finished boards, as supplied by the board manufacturer, and are expressed in inches and millimeters.

3 OUTSIDE CONFIGURATION

Tolerances or limits for length, width, thickness, warpage, slots, notches, cutouts, straightness, parallelism, and squareness are specified in the following paragraphs.

3.1 LENGTH AND WIDTH

Unless otherwise specified, the tolerances for length (measured perpendicular to fingers) and the tolerances for width (measured parallel to fingers) shall be ±0.020 inch (±0.51 mm) on the finished circuit size, disregarding nonfunctional test and tooling areas.

Unless otherwise specified, the tolerance for assembly board length or width when measured to a nonfunctional test or tooling area outside the finished circuit perimeter is ±0.031 inch (±0.79 mm).

3.2 THICKNESS—FINGERLESS BOARDS

Refer to the text under heading 10 for thicknesses of ML and MSL boards.

Unless otherwise specified, board thickness when measured over etch inclusive of all plating shall be as follows.

a. The acceptable maximum board thickness for a nominal 0.061 fingerless board shall be 0.070 inch (1.78 mm), and the acceptable minimum thickness shall be 0.052 inch (1.32 mm).

b. For other fingerless boards, the thickness tolerances shall be ±10 percent of the nominal overall board thickness or ±0.007 inch (±0.18 mm), whichever is greater.

NOTE

The maximum overall PWB thickness inclusive of soldermask shall be the overall thickness measured over etch inclusive of all plating plus 0.004 inch (0.10 mm) per soldermasked side.

3.3 THICKNESS—PWBS WITH FINGERS

Unless specified otherwise, layer construction/layup detail drawings for single-sided /double-sided with PTH boards with fingers are as follows.

C-MD-ELEN627-00-DBU	*Layer Construction, Board, Single-Sided, Non-PTH*
C-MD-ELEN628-00-DBU	*Double-Sided, Non-PTH*
C-MD-ELEN629-00-DBU	*Layer Construction, Board, Double-Sided, PTH*
C-MD-ELEN630-00-DBU	*Layer Construction, Board, 4-Layer*
D-MD-ELEN631-00-DBU	*Standard Layer Construction Detail, 6-Layer Board*
D-MD-ELEN632-00-DBU	*Standard Layer Construction Detail, 8-Layer Board*
D-MD-ELEN633-00-DBU	*Generic Layer Construction VAXBI Module Detail—10-Layer Board*
D-MD-ELEN635-00-DBU	*XMI Module Detail—10-Layer Module Construction*

NOTE

These detail drawings are contained in *EL-ENPCB-02 PC Board Engineering Handbook—Layer Construction Drawings.*

For single-sided/double-sided with PTH boards with fingers referencing these drawings in their documentation, overall board thickness/tolerances (measured over etch inclusive of all platings) and dielectric thickness/tolerances shall be as shown in the drawings, unless specified otherwise. Copper foil thicknesses/tolerances in the drawings are based on raw stock only.

Table 2: Copper Foil Thicknesses

Copper Foil Weight (oz/ft^2)	Copper Foil Thickness Raw Stock (inches)	Minimum Copper Foil Thickness (After PWB Processing) (inches)
1/2	0.0007 ± 0.0002	0.0003
1	0.0014 ± 0.0002	0.0010
2	0.0028 ± 0.0003	0.0022
3	0.0042 ± 0.0004	0.0036

For fingerless single-sided/double-sided with PTH boards, referring to the layer construction drawings listed under this subhead. The copper and dielectric thicknesses/tolerances shall be as shown in the drawings unless specified otherwise. Copper foil thicknesses/tolerances in the drawings are based on raw stock only. The minimum copper foil thickness after PWB processing is given in Table 2.

NOTE

The maximum overall PWB thickness inclusive of soldermask shall be the overall thickness measured over etch inclusive of all plating plus 0.004 inch (0.10 mm) per soldermasked side.

3.4 WARPAGE

When measured in accordance with Appendix C, the maximum warpage (bow or twist) shall be as listed in Table 3.

Table 3: Maximum Warpage

Nominal Board Thickness[1]		Maximum Warpage Ratio
inch	mm	inch/inch
Less than 0.031	Less than 0.79	0.015
0.031—0.063	0.79—1.6	0.010
Over 0.063—0.094	Over 1.6—2.39	0.007
Over 0.094—0.250	Over 2.39—6.3	0.005

[1]See DEC STD 176-6 for single-sided boards.

3.5 SLOTS, NOTCHES, AND CUTOUTS

Unless specified otherwise, the dimensional tolerances for slots, notches, and cutouts shall be ±0.020 inch (±0.51 mm) and the locational tolerances for these items shall be ±0.020 inch (±0.51 mm).

3.6 STRAIGHTNESS, PARALLELISM, AND SQUARENESS

For board edges, the straightness, parallelism, and squareness shall not exceed 0.03 inch per foot (2.1 mm per m).

4 BASE MATERIAL VISUAL CHARACTERISTICS

Acceptable and unacceptable surface conditions are specified in the following sections.

4.1 SURFACE AND SUBSURFACE CONDITIONS

Unclad and nonplated surfaces of base materials may exhibit weave texture, regardless of the area it covers, provided the reinforcement fibers are completely covered with resin. Unclad and nonplated surfaces of base materials may exhibit weave exposure, provided that the total area is not greater than 5 percent of the board area, and weave exposure does not span more than 25 percent of the distance between adjacent conductors.

Internal or external discolorations that are nonconductive, nonnutrient, and related to approved processing, such as minor scorching, are acceptable. There should be no indication of delamination, measling, charring, blistering, or lifting of circuit foil that may affect form, fit, function, reliability, serviceability, or processability of a circuit board.

Furthermore, there shall be no detrimental foil-bonding agent, foil treatment, or foreign materials embedded in the dielectric.

4.2 CHIPS, CRACKS, FIBERS, AND HALOING—LAMINATE

Maximum allowable extensions from different edges are listed in Table 4.

Table 4: Maximum Allowable Extensions—Laminate

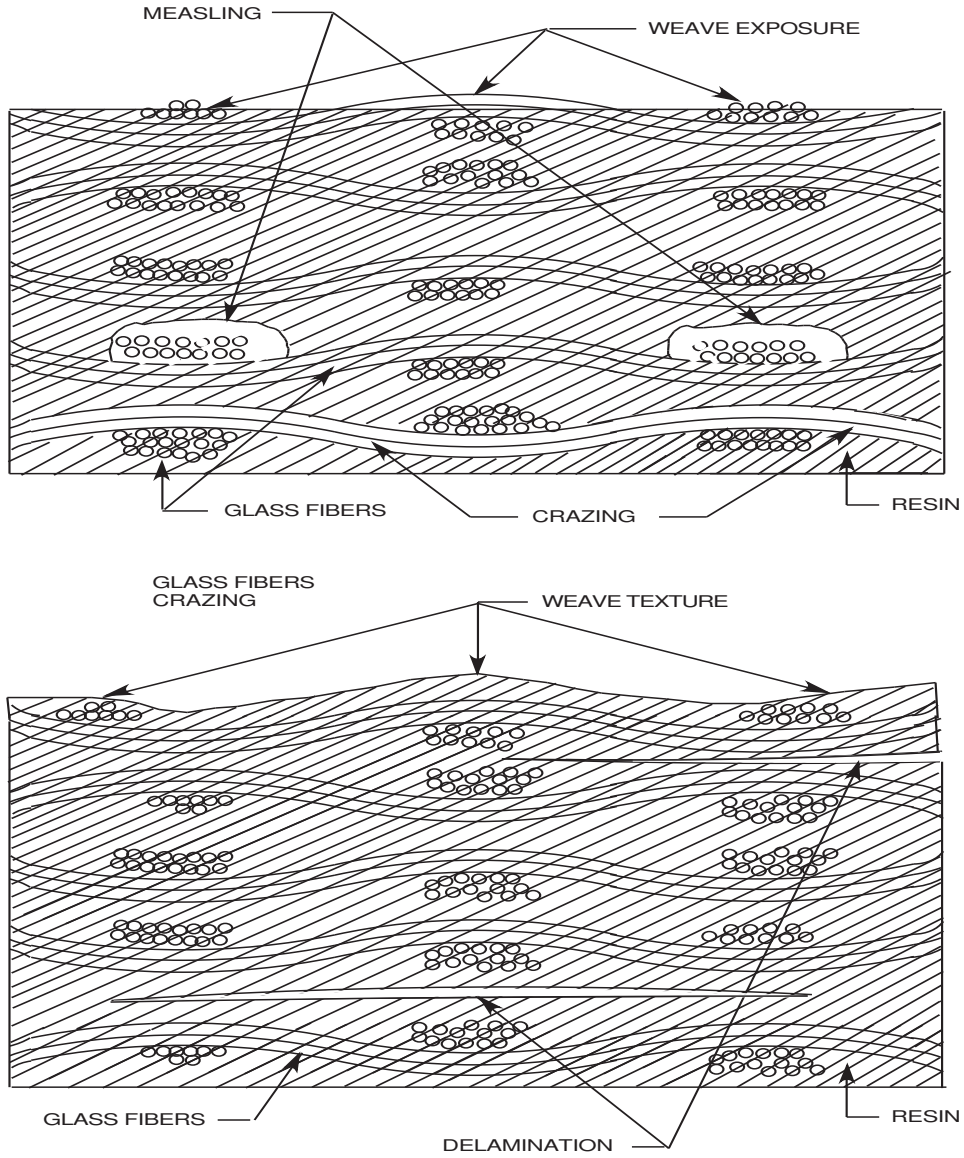
Condition	Board		Slot, Notch, or Cutout	
	inches	mm	inches	mm
Chips, cracks, fibers	0.010	0.25	0.010	0.25
Haloing*	0.010	0.25	0.010	0.25

* For boards with a nominal thickness above 0.06 inch (1.52 mm), haloing may extend to 0.03 inch (0.76 mm) provided it is not closer than 0.010 inch (0.25 mm) from any other board feature (such as a pad or conductor).

4.3 DELAMINATION, CRAZING, AND MEASLING

Delamination shall not extend in more than 15 percent of the nominal board thickness from the board edges. Delamination, crazing, and measling shall not bridge more than 25 percent of the distance between adjacent conductors and shall not reduce the spacings between conductors below minimums. Delamination, crazing, and measling shall not be greater than 0.065 inch (1.65 mm) in diameter or cover more than 1 percent of the total circuit area. Delamination shall not propagate as a result of thermal testing, such as thermal stress/shock, assembly processing, and rework.

Figure 2: Measling, Crazing, and Delamination



5 HOLES

The criteria for nonplated and plated holes are as follows.

5.1 NONPLATED DRILLED AND PUNCHED HOLES

Requirements are specified in the following paragraphs for nonplated hole diameters, pattern accuracy, chips, cracks, fibers, haloing, delamination, and missing and extra holes.

5.1.1 Nonplated Hole Diameters

Unless otherwise specified, drilled, punched, or routed hole diameter tolerances shall be as listed in Table 5 and shall not contain any plating. The preferred method of measurement is using pin gauges.

Table 5: Nonplated Hole Diameters

Nominal Diameters		Tolerances	
inches	mm	inches	mm
Under 0.125	Under 3.18	±0.003	±0.08
0.125 to 0.250	3.18 to 6.35	±0.005	±0.13
0.251 and over	6.38 and over	± 0.020	±0.51

NOTE

Nominal tooling hole diameter and tolerances are 0.250 inch, +0.000 inch/-0.003 inch (6.35 mm, +0.000 mm/-0.08 mm); 0.157 inch, ±0.002 inch (3.99 mm, ±0.05 mm).

5.1.2 Chips, Cracks, Delamination, Fibers, Haloing— Drilled and Punched Holes

Maximum allowable extensions from drilled and punched hole edges are given in Table 6.

Table 6: Maximum Allowable Extensions—Drilled/Punched Holes

Condition	inches	mm
Chips	0.005	0.13
Cracks	0.005	0.13
Delamination[1]	0.010	0.25
Fibers	0.005	0.13
Haloing	0.010	0.25

[1]Delamination may not be located within 0.010 inch (0.25 mm) of any other functional board feature.

5.1.3 Missing and Extra Holes

Missing holes are not acceptable. Extra holes are acceptable through the base material or through a portion of a conductive pattern if they do not violate the minimum line width. Extra holes must have no electrical effect on the conductive pattern.

5.2 PLATED-THROUGH HOLES (PTH)

Requirements are specified in the following sections for PTH diameters, plating thicknesses, and other characteristics.

5.2.1 Plated-Hole Diameters

Unless specified otherwise, PTH finished-hole size (FHS) and diameter tolerances shall be according to Table 7. The preferred method of measurement is with pin gauges.

NOTE

Table 7 shows practical metric equivalents, not mathematically converted measurements. This table takes into consideration both U.S. customary and metric drill sizes. For hole sizes not shown in Table 7, see Appendix E.

Table 7: PTH Diameters and Tolerances*

Nominal Diameter		Tolerances	
inches	mm	inches	mm
	Component Holes		
0.032 **	0.81	±0.003	+0.09/-0.08
0.034 **	0.86	±0.003	+0.09/-0.08
0.038	0.97	+0.004 -0.003	+0.10 -0.08
0.041	1.04	+0.002 -0.003	+0.05 -0.08
0.042 ***	1.07	+0.005 -0.003	+0.13 -0.08
	All Other Holes*		
0.063 and under	1.60 and under	±0.004	±0.10
Over 0.063 to 0.250	Over 1.60 to 6.35	±0.005	±0.13

Notes to Table 7.

* PTH diameter and tolerance for via interconnections shall be nominal plus 0.003 with no minimum. All other plating thickness minimums and characteristics apply.

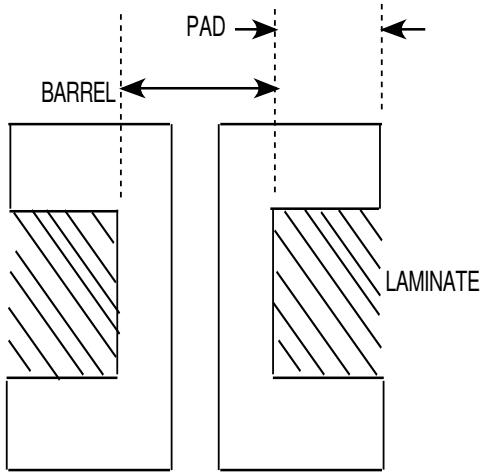
** Typically used for 90-0149-00 stake pin. This pin is used for double-sided PWBs equal to or less than 0.093 inch (2.36 mm) nominal thickness. Double-sided PWBs of 0.062 inch (1.57 mm) nominal thickness require a 0.032 inch (0.81 mm) nominal finished hole size for this pin. Double-sided PWBs 0.093 inch (2.36 mm) nominal thickness require a 0.034 inch (0.86 mm) nominal finished hole size for this pin.

*** Nominal hole sizes for standard density designs prior to March 1986 were 0.042 inch (1.07 mm). These are not required for new designs. The nominal hole size for standard density and high density product is now 0.038 inch (0.97 mm). The tolerance for the nominal 0.038 inch (0.95 mm) hole size applies.

5.2.2 Plating Thicknesses

Plating thicknesses shall be measured at 400X via microsection in accordance with text under subhead 2.1.1 of IPC-TM-650. Microsection sample coupons shall be taken from three locations diagonally across the board (one coupon from each corner and one in the center). These microsection coupons shall contain plated-through holes representing both the predominate hole size as well as the minimum hole size. For the purpose of determining PTH plating thickness and quality characteristics, the regions of the PTH that are defined as the barrel and pad are shown in Figure 3.

Figure 3: Barrel and Pad



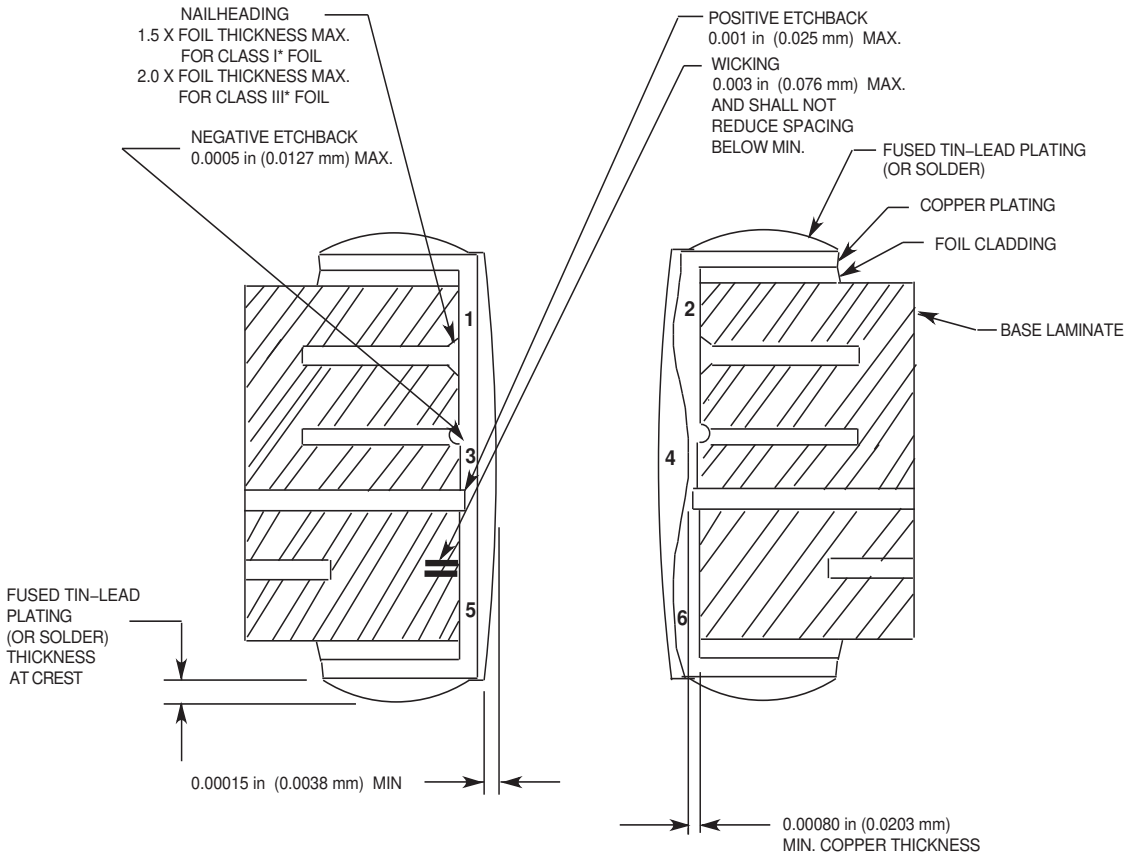
For a given PTH, the minimum copper plating thickness in the barrel is determined by scanning both sides of the PTH wall and locating the absolute minimum copper thickness. Pinholes, voids, pits, and nodules are excluded from this measurement. No PTH shall exhibit less than 0.00080 inch (0.0203 mm) minimum copper thickness. See Figure 4.

For a given PTH, the thickness of fused tin/lead (or solder) shall be 0.00015 in (0.00381 mm) minimum when measured at the crest. The crest on the PTH is determined by scanning the pad surface on both sides of the PTH and locating the region of maximum thickness, which is the crest. For the barrel of the PTH, the crest is determined by scanning both sides of the PTH wall and locating the region of maximum thickness. There shall be coverage of the entire PTH and knee region with tin/lead (or solder). There shall be no exposed copper that exceeds the void defect criteria. See text under subhead 5.2.3.

NOTE

Test coupons are used for board manufacturing process controls only. Accept/reject decisions are based on testing of actual board circuitry.

Figure 4: Plating Thickness and Quality



*ANSI/IPC–CF–150 type ED

5.2.3 Other PTH Characteristics

The following shall be determined via microsectioning and appropriate magnification. Refer to the text under subhead 2.4 for more information on microsectioning and magnification.

a. Plating nodules and glass fiber protrusions are acceptable if they do not reduce the hole diameter and plating thickness below the minimum specified.

b. Plating voids are acceptable under the following conditions.

   1. There are no more than three voids per hole.
   2. The maximum allowable void dimension in any direction is 0.003 inch (0.076 mm).
   3. Circumferential voids are not acceptable.
   4. They are not located at foil/plating interfaces.
   5. Plated-through holes that have no pads or pads on one side do not have to meet the minimum hole-plating requirements.

c. Resin smear on the outer-layer foil at the hole edge is acceptable if it does not interrupt electrical continuity. There shall be no evidence of resin smear at the interface between the inner-layer foil and the PTH plating.

d. Cracks or separations in the PTH plating or inner-layer foil/plating interfaces (post separation) are not acceptable.

e. Cracks are permissible in the outer-layer copper foil for IPC-CF-150 *Copper Foil For Printed Wiring Applications* Electrodeposited Class I and III foils provided they do not extend into the plated copper.

   For IPC-CF-150 Electrodeposited Class I foils, cracks in the inner-layer foil are not acceptable.

   For IPC-CF-150 Electrodeposited Class III (high temperature elongation) foils, cracks are permitted in the inner-layer foil under two conditions:

   i They are less than or equal to 25 percent of the foil thickness.

   ii They do not propagate as a result of thermal testing, such as thermal stress/shock, assembly processing, and rework. See Figures 5 and 6.

f. For PWBs using IPC-CF-150 Electrodeposited Class I foil, nail heading is acceptable if it is equal to or less than 1½ times the foil thickness.

g. For PWBs using IPC-CF-150 Electrodeposited Class III foil, nail heading is acceptable if it is equal to or less than two times the foil thickness. See Figure 4.

h. For PWBs equal to or greater than four layers, *negative etchback* of copper foil behind the plane of the PTH wall shall not exceed 0.0005 inch (0.013 mm). Lateral removal of base material from the PTH wall *positive etchback* shall not exceed 0.0010 inch (0.025 mm). Refer to Figure 4.

i. For PWBs equal to or greater than four layers, *wicking* of plating chemistry may extend laterally 0.003 inch (0.08 mm) maximum into the laminate providing it does not reduce conductor or dielectric spacing below minimum. Refer to Figure 4.

j. For PWBs equal to or greater than four layers, delamination shall not span more than 25 percent of the distance between adjacent conductors or PTHs. Delamination shall not reduce spacings between conductors below minimum. Delamination shall not propagate as a result of thermal testing, such as thermal stress/shock, assembly processing, and rework. When evaluated *as received* and/or after thermal stress, as stated in subhead 7.5 of this standard, the maximum *pad lifting* from the base material to the lower edge of the lifted pad shall be a maximum of 0.003 inch (0.08 mm). In addition, there shall be a minimum of 10 percent of the pad width bonded to the laminate on at least one side of the hole. Refer to Figures 5 and 6.

k. For printed-wiring boards cross-sectioned in the *as received* condition, separation of the base material from the plating in the hole wall (resin recession) *is acceptable,* provided all of the following criteria are met. Refer to Figures 5 and 6 for further illustration.

   1. The maximum horizontal distance measured from the base material to the copper plating is less than or equal to 0.003 inch (0.08 mm).

   2. The maximum vertical length is less than or equal to 40 percent of the cumulative dielectric thickness of the base material (overall metal-to-metal thickness minus all foil and plating thicknesses).

3. The separation is less than or equal to half the circumference of the hole when viewed in a horizontal microsection.

Figure 5: Plated-Through Hole Evaluated in *As Received* Condition

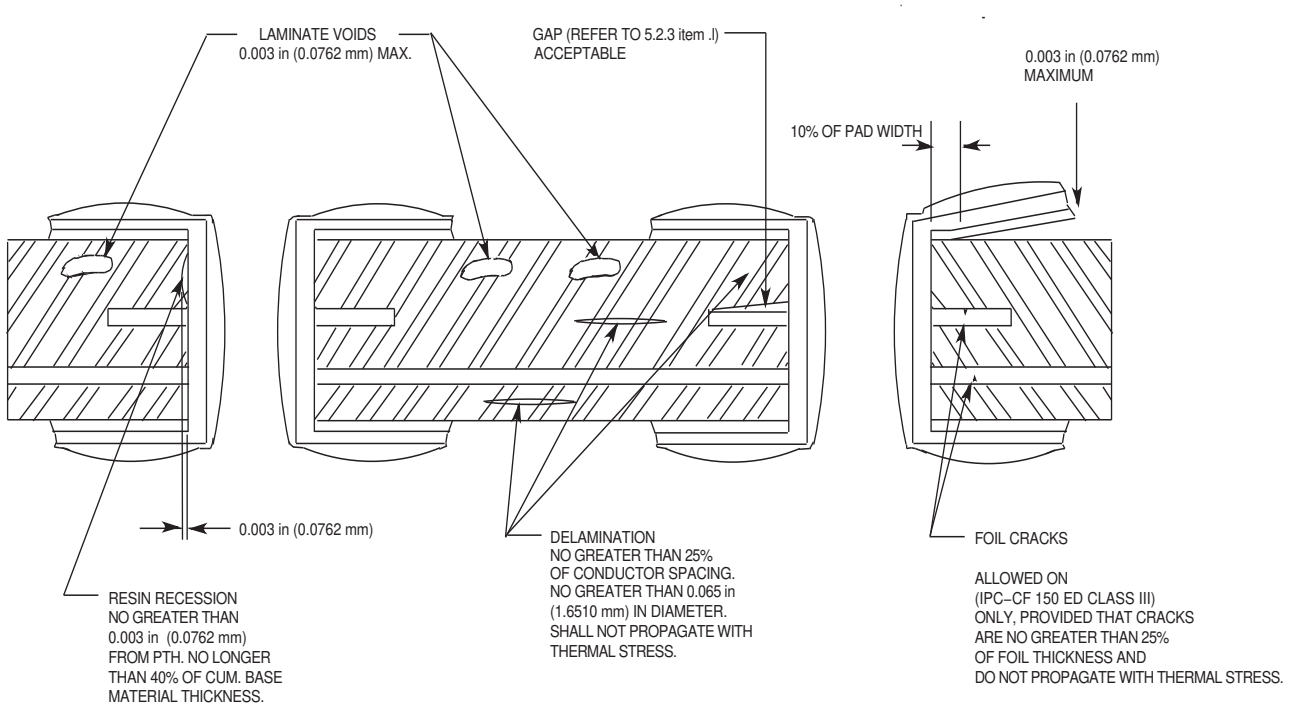
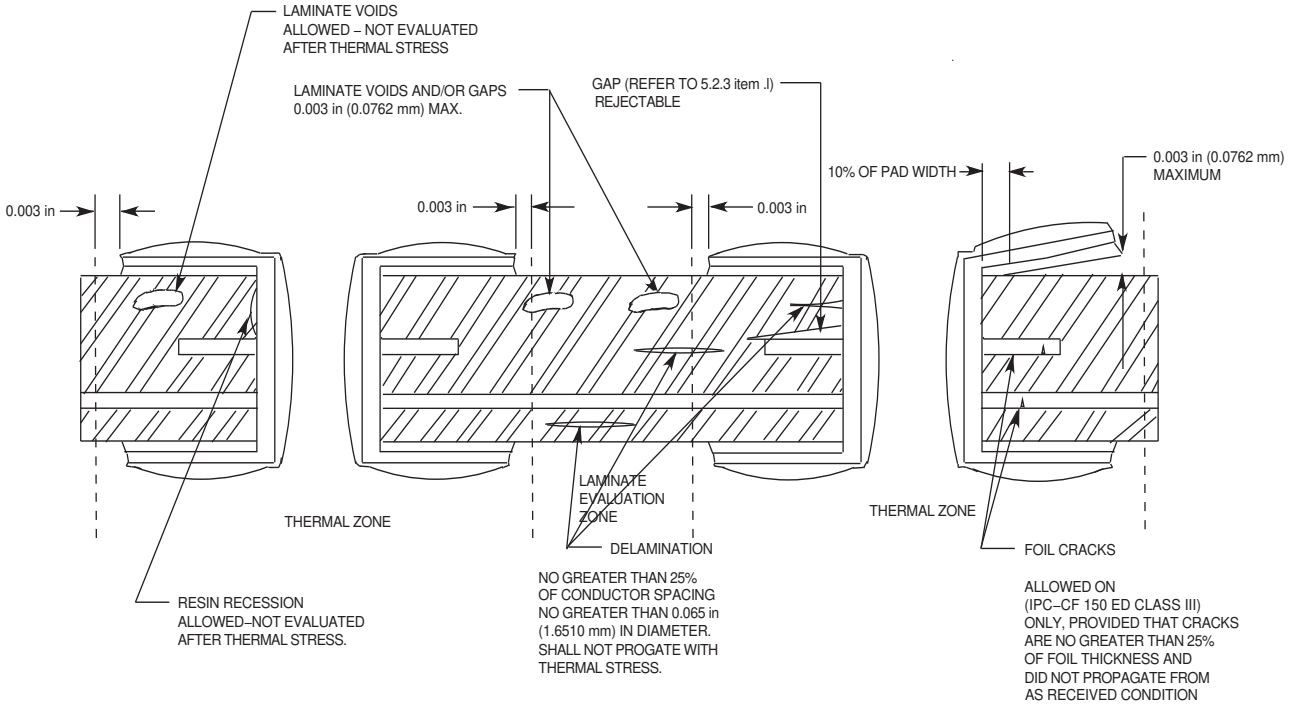


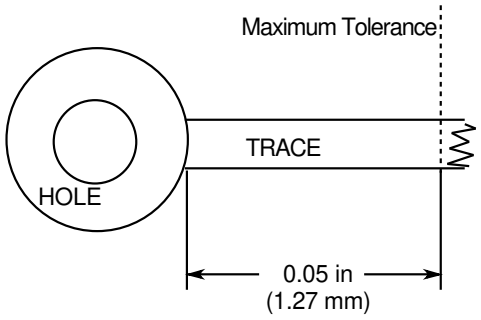
Figure 6: Plated-Through Hole Evaluated After Thermal Stress



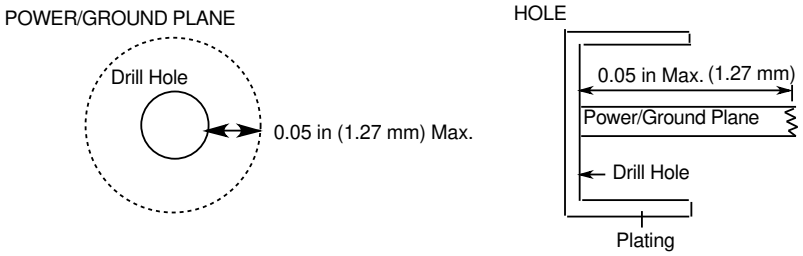
l. When evaluated in the *as received* condition using horizontal or vertical microsection techniques, gaps between inner-layer copper foil and *B-stage* areas are permitted under the following conditions.

1. The maximum extent of gaps created as a result of lateral removal of inner-layer oxide *Pink Ring* does not exceed:

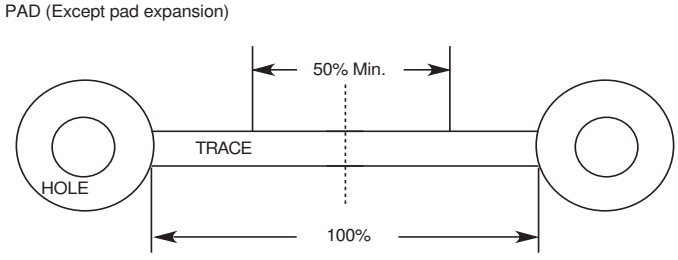
a. 0.05 inch (1.27 mm) down a signal trace as measured from the signal pad diameter (not inclusive of pad expansion).



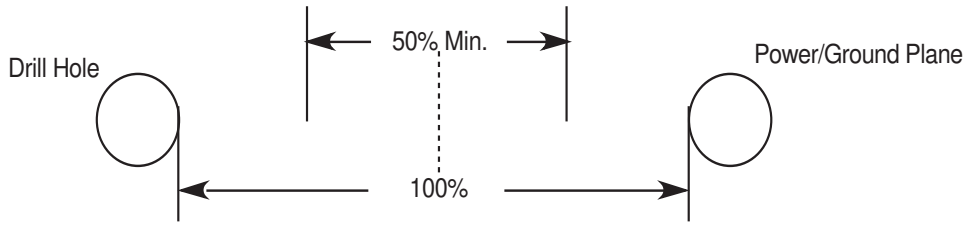
b. 0.05 inch (1.27 mm) beyond the drilled hole edge for *direct* or *thermal relief* PTH connections to inner-layer power/ground planes.



c. Fifty percent of the distance along a signal trace connected by two or more signal pads as measured from the signal pad diameters (not inclusive of pad expansion).



d. Fifty percent of the distance between adjacent power and/or ground features as measured from the drilled hole edges.



The extent of lateral oxide removal shall be determined by measuring the total distance from the reference points above, along the region(s) of oxide removal, to the point(s) where the unaffected oxide begins.

2. The maximum extent of gaps **not** created as a result of lateral removal of inner-layer oxide *Pink Ring* shall not exceed the inner-layer pad diameter.
3. The extent of any gap shall not propagate after thermal stress testing, as stated in subhead 7.5 of this document.
4. There are no plating voids, folds, or plating thickness reductions below minimum tolerances adjacent to any gap area.
5. PTH plating adjacent to any gap area shall not crack or separate after thermal stress testing, as stated in text under subhead 7.5 of this document.
6. There is no entrapment of foreign materials or plating solutions inside any gap area (such as *outgassing* or *blow holes* following thermal stress testing).

m. For printed-wiring boards equal to or greater than four layers, the acceptance criteria for laminate voids is as follows.

1. When evaluated in the *as received* condition, laminate voids with longest dimension greater than 0.003 inch (0.08 mm) are not acceptable.
2. When evaluated after thermal stress as stated in text under subhead 7.5 of this document, distinction between acceptable and rejectable laminate voids shall be based on the concept of a *thermal zone* and a *laminate evaluation zone*. The delineation between the *thermal zone* and the *laminate evaluation zone* is determined by imaginary lines drawn parallel to the PTH axis at a distance of 0.003 inch (0.08 mm) beyond the edges of the top and bottom outer-layer pad diameters on each side of the PTH view. On each side of the PTH view, the region extending from the wall of the PTH to the imaginary lines is defined as the *thermal zone*. The regions beyond the imaginary lines extending to the *thermal zone* of the nearby PTHs is defined as the *laminate evaluation zone*. The criteria for resin recession and laminate voids following thermal stress is as follows.

   a. Resin recession and laminate voids shall not be evaluated within the *thermal zone* and shall be deemed acceptable if noted.

   b. Laminate voids that extend into or reside within the *laminate evaluation zone* are evaluated and shall not exceed 0.003 inch (0.08 mm) in the longest dimension. Refer to Figure 7.

5.3 HOLE LOCATION ACCURACY (HLA)

Hole Location Accuracy (HLA) shall be determined with a properly calibrated, coordinate measuring machine with suitable accuracy, precision, and repeatability. All measurements shall be performed on finished product from Side 1. For a multiple circuit board, HLA shall be assessed on an individual circuit basis (not cumulative). HLA shall be measured from an absolute reference datum (typically a dimensioned hole) to any plated or nonplated hole including assembly rezero holes. Defer to the rezero hole if the datum is not on print. The assembly rezero holes are used by Digital Module Assembly as zero reference locations for autoinsertion. The rezero holes are identified on the assembly board drawing and shall meet the following requirements.

a. Drilled during the same *setup* as the drilling of conductive pattern holes.

b. Typically the same diameter as the predominant drilled hole size. However, diameters should not exceed the range 0.04 inch (1.0 mm) minimum to 0.05 inch (1.27 mm) maximum.

c. The surface edges and inner diameter shall be clear of all foreign material and shall not be damaged or distorted in any way.

d. May be plated-through providing requirements a through c are met.

The HLA for holes that are drilled shall be:

Geometric location tolerance (GLT): ± 0.003 inch (± 0.08 mm)
True position diameter (TPD): 0.0085 inch (0.22 mm)

The HLA for holes that are *punched* shall be 0.014 inch (0.36 mm) TPD, ±0.005 inch (±0.13 mm) GLT. Use the same procedure for determining hole location accuracy as described for drilled holes.

Refer to Appendix B for calculation of TPD/GLT.

6 CONDUCTORS AND PADS

Conductor widths and spacing, pad diameters, annular rings, plating thicknesses, edge characteristics, and other characteristics utilizing 1 oz. copper are specified in the following sections.

6.1 CONDUCTOR WIDTHS (INNER AND OUTER LAYER)

Unless specified otherwise, when measuring for edge definition in accordance with IPC-TM-650, the minimum conductor widths measured at the base laminate – foil (plating) interface shall be in accordance with Table 8.

Table 8: Conductor Widths

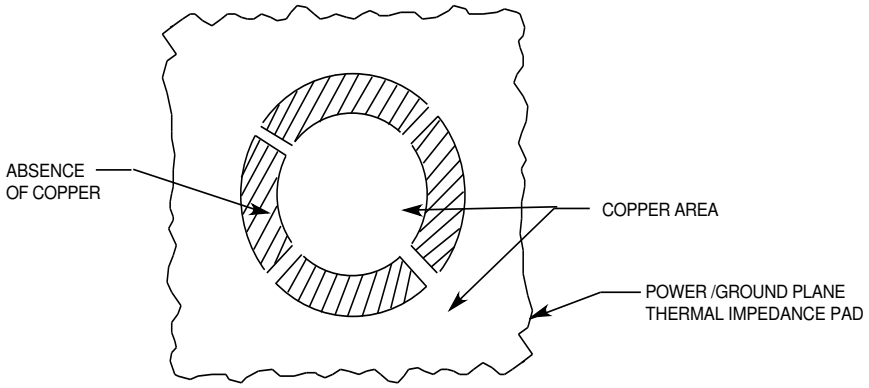
Nominal Width		Minimum Width[1]
in	mm	
> 0.010	> 0.25	Nominal minus 0.003 in (0.08 mm)
0.006 through 0.010	0.15 through 0.25	Nominal minus 0.002 in (0.05 mm)
< 0.006	< 0.15	Nominal minus 0.001 in (0.03 mm)

[1] For product using 2 oz. base copper foil with conductor lines greater than 0.015 in (0.38 mm), the minimum conductor width shall be nominal minus 0.005 in (0.13 mm).

6.1.1 Thermal Impedance Conductors (Legs)

The sum total of the thermal impedance conductor widths that connect to the power/ground planes shall be 0.030 inch (0.76 mm) minimum.

Figure 7: Typical Power/Ground Plane Thermal Impedance Pad



6.2 SPACING (INNER AND OUTER LAYER)

Minimum conductor-to-conductor, conductor-to-pad, and pad-to-pad spacing for all layers shall be in accordance with Table 9.

Table 9: Spacing

Nominal Spacing		Minimum Spacing[1]
in	mm	
> 0.020	> 0.51	Nominal minus 0.005 in (0.13 mm)
> 0.010 through 0.020	0.25 through 0.51	Nominal minus 0.004 in (0.10 mm)
> 0.008 through 0.010	0.20 through 0.25	Nominal minus 0.003 in (0.08 mm)
0.005 through 0.008	0.13 through 0.20	Nominal minus 0.002 in (0.05 mm)
0.005	0.13	Nominal minus 0.001 in (0.03 mm)

[1] For product using 2 oz. base copper foil with spacing greater than 0.013 in (0.33 mm), the minimum spacing shall be nominal minus 0.006 in (0.15 mm).

6.3 PAD DIAMETERS (INNER AND OUTER LAYER)

Minimum pad diameters shall be in accordance with Table 10.

Table 10: Pad Diameters

Nominal Diameter		Minimum Diameter[1]
in	mm	
> 0.040	> 1.02	Nominal minus 0.005 in (0.13 mm)
0.025 through 0.040	0.64 through 1.02	Nominal minus 0.003 in (0.08 mm)
< 0.025	< 0.64	Nominal minus 0.002 in (0.05 mm)

[1] For product using 2 oz. base copper foil with pads less than 0.035 in (0.89 mm), the minimum diameter shall be nominal minus 0.006 in (0.15 mm).

6.4 ANNULAR RINGS—MAXIMUM ALLOWABLE MISREGISTRATION FOR MSL AND NON-MSL TECHNOLOGIES

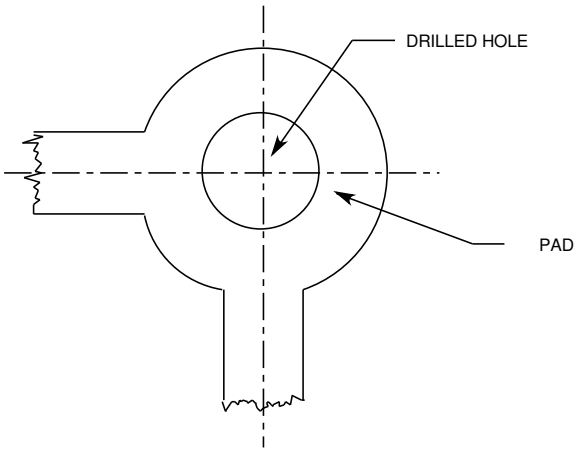
The following conditions are the maximum allowable for both MSL and Non-MSL technologies.

6.4.1 Inner Layer and Outer-Layer Features

Acceptability levels for inner-layer and outer-layer annular rings for all holes are specified as follows. Hole location should meet the criteria in the text under subhead 5.3.

a. **Preferred**

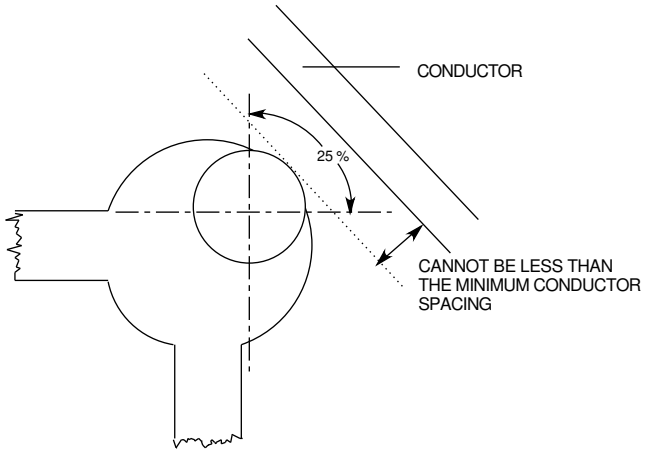
Figure 8: Preferred Hole-to-Pad Registration



Hole concentric with the pad.

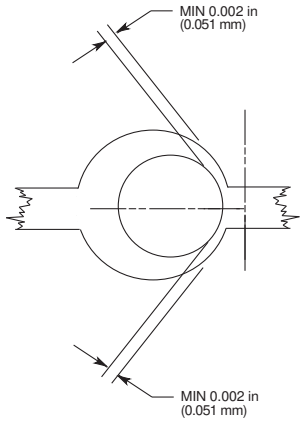
b. **Maximum Acceptable Breakout**

Figure 9: Maximum Hole-to-Pad Breakout



The maximum allowable hole-to-pad breakout shall be 25% of the drilled hole circumference *OR* the minimum conductor-to-conductor spacing, whichever is less.

Figure 10: Minimum Clearance Between Hole and Conductor-Pad Interface —Without Elongated Pad

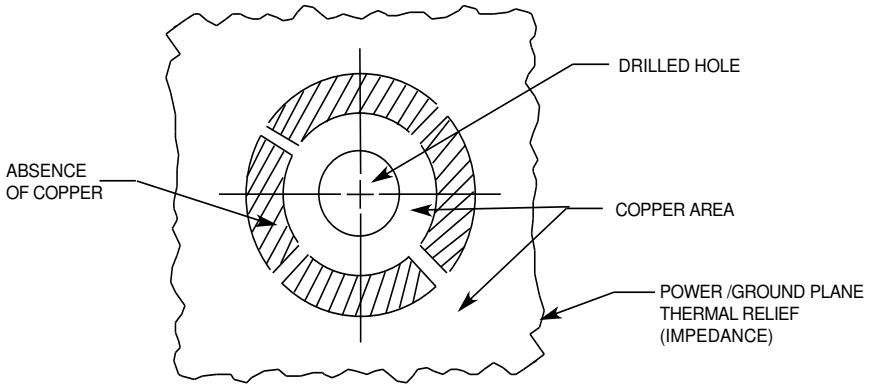


Minimum 0.002 inch (0.051 mm) between hole and both sides of conductor-pad interface.

6.4.2 Power and Ground Planes or Thermal Impedance Pad Areas

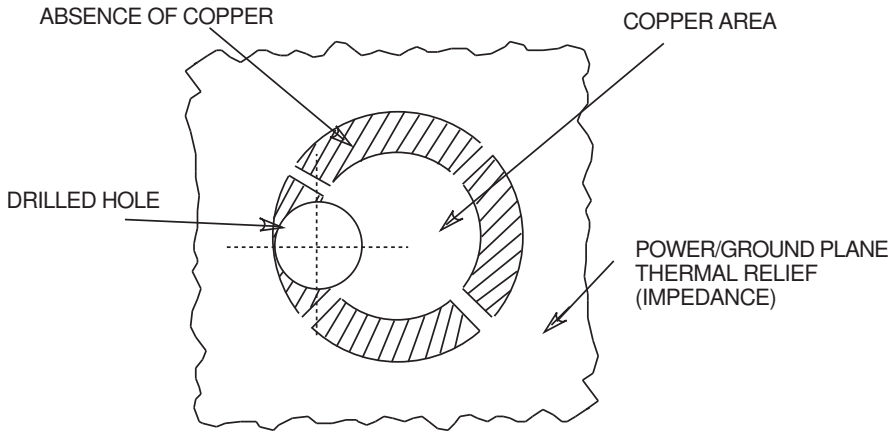
a. **Preferred**

Figure 11: Preferred Hole-to-Pad Registration—Thermal Impedance Pads



Hole concentric with the inner-layer clearance.

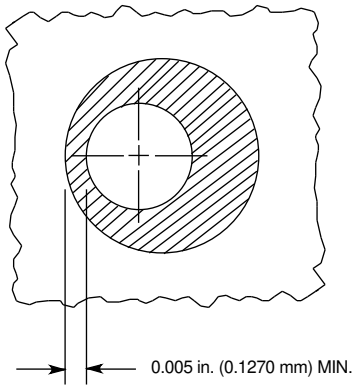
Figure 12: Maximum Allowable Breakout of Hole-to-Thermal Impedance Pad



Hole breakout of inner pad but tangent to inner-layer plane. A minimum of 0.030 inch (0.76 mm) copper must remain intact.

b. **Acceptable**

Figure 13: Minimum PTH-to-Inner Layer Plane Clearance



Hole 0.005 inch (0.13 mm) from clearance-hole edge.

6.5 PLATING THICKNESSES—ETCH LINES

Using microsectioning and appropriate magnification, the minimum conductor plating thicknesses at the crest shall be as indicated in Figure 14, unless otherwise permitted. See text under subhead 2.4.

Figure 14: Plating Thickness—Etch Lines

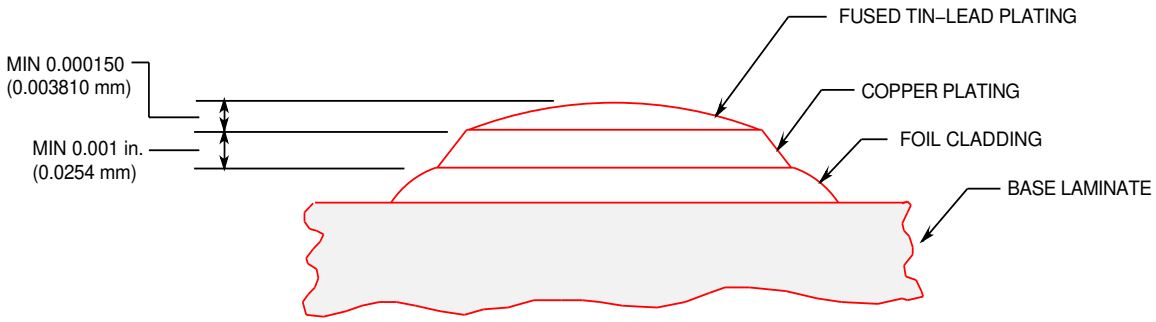


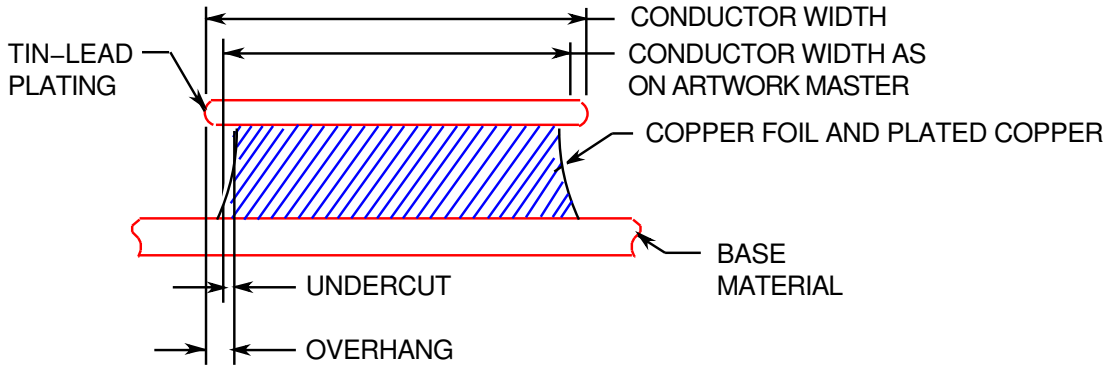
Table 11: Plating Thickness—Etch Lines

Plating Material	Minimum Thickness
Electroless copper	Sufficient for subsequent copper electroplating.
Electrolytic copper	0.001 inch (0.03 mm).
Fused tin-lead and solder	0.00015 inch (0.00381 mm) crest. Total coverage on conductor/pad sidewall preferred but not required.

6.6 ETCH CHARACTERISTICS

As determined via microsectioning and appropriate magnification, defined in text under subhead 2.4, undercutting at all edges shall not exceed the total thickness of the copper foil and the plated copper.

Figure 15: Etch Undercutting



6.7 OTHER ETCH CHARACTERISTICS

Other characteristics include blisters, breaks, delaminations, inclusions, nodules, nicks, scratches, pits, dents, test probe marks, and voids (see Figure 16). Some of these visual imperfections in conductors and pads are permitted within the maximum limits specified below.

a. Blisters, breaks, and delaminations (lifted conductors or peeling) are not acceptable under any circumstances.

b. Nicks, scratches, pits, dents, test probe marks, inclusions, and voids are acceptable under the following circumstances.

   1. Electrical and mechanical integrity of interconnect is maintained and performance is not affected.

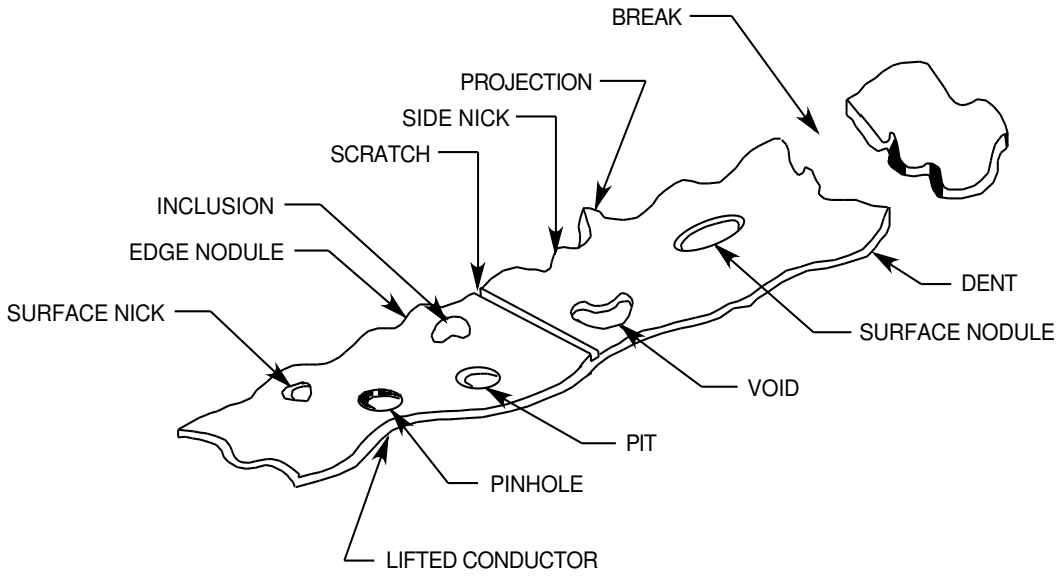
   2. For an isolated indentation (0.5 inch maximum total length along a conductor run), the minimum acceptable line width shall be no less than 85 percent of the minimum width specified in the text under subhead 6.1.

   3. Where there is exposed copper on the surface, refer to subhead 9.9.4.

c. Conductor edge nodules and projections are acceptable if they do not cause the affected conductors or pads to violate the minimum spacing or conductor requirements.

d. Isolated unetched protrusions or nodules with exposed copper are acceptable if they do not violate spacing requirements and are not in the finger contact area.

Figure 16: Etch Imperfections



7 PLATING CHARACTERISTICS

The following describes the required criteria related to Plating characteristics.

7.1 TIN-LEAD PLATING (FUSED)

Fusing of tin-lead plating is required on all solderable surfaces. All nonterminal areas of conductors and power/ground planes may be dewetted. All tin-lead plated surfaces shall be 50 to 70 percent tin (30 to 50 percent lead) content. The fused tin-lead shall be 0.000150 inch (0.0038 mm) thick minimum when measured at the crest. Total coverage of conductor/pad sidewall is preferred but not required.

As determined by microsectioning and appropriate magnification (see text under subhead 2.4), the PTH and pad shall meet the requirements under subheads 5.2.2 and 5.2.3.

7.2 ADHESION

When PWBs are inspected for plating adhesion using the tape test described in text under subhead 2.4.1 of IPC-TM-650, no parts of the conductive pattern, including outgrowth, shall be removed from the boards.

7.3 BOND STRENGTH (TERMINAL PULL STRENGTH)

When tested in accordance with subhead 2.4.21 of IPC-TM-650, the plated-through hole shall withstand 20 pounds (90 N) of pull or 2000 psi (14 N/mm^2), whichever is less. The plated hole and connected conductor or pad shall not be loosened. A failure occurs when the PTH and/or terminal area (pad) is loosened or lifted with soldered wire attached.

7.4 SOLDERABILITY

Holes and terminal areas that will be soldered shall demonstrate at least 95 percent wetting with 5 percent unconcentrated dewetting and pinholing allowed; there shall be no evidence of nonwetting. All nonterminal areas of power and ground planes may be unfused and may be dewetted. Refer to IPC-S-804 *Solderability Test Methods for Printed Wiring Boards*.

Solderability tests shall be in accordance with IPC-S-804. Regardless of the test method used, the following shall occur.

a. Proper wetting of the surface, hole wall, and terminal area.

b. No blistering, delamination (lifted conductors) or other forms of degradation of the conductive pattern.

7.5 THERMAL STRESS (PLATED-THROUGH HOLES)

After a PTH specimen is tested in accordance with Appendix D of this standard, there shall be no blistering and no delamination or additional measling in the base material. Pinpoint delamination is acceptable.

Microsectioned specimens under appropriate magnification shall meet the requirements specified in text under subhead 5.2.3. See text under subhead 2.4.

8 FINGERS

Criteria for plating thickness, surface finish, porosity, unused fingers, adhesion, length, width, spacing, beveling, edge taper, and other characteristics are specified in the following sections.

8.1 PLATING THICKNESSES

As determined on a beta backscatter instrument or equivalent, minimum finger-plating thicknesses for edge card pluggable modules shall be 0.00003 inch (0.0008 mm) electrolytic gold over nickel and 0.00010 inch (0.00254 mm) electrolytic nickel over copper, unless specified otherwise. Electrolytic gold is measured at a minimum density, as plated, of 17 gm/cm^3. Electrolytic gold over copper is not allowed. See Figure 20.

As determined on a beta backscatter instrument or equivalent, minimum finger-plating thicknesses for non-edge card pluggable modules (for example, zero insertion force tabs, and so forth) shall be 0.00005 inch (0.00127 mm) electrolytic gold over nickel and 0.00010 inch (0.00254 mm) electrolytic nickel over copper, unless specified otherwise. Electrolytic gold is measured at a minimum density, as plated, of 17 gm/cm^3. Electrolytic gold over copper is not allowed. See Figure 20.

8.2 SURFACE FINISH

As determined with a calibrated profilometer or similar instrument, electroplated gold surface finish, measured in the direction of the connector contact insertion, shall be a maximum of 0.00006 inch (0.0015 mm) arithmetic average. When determining the acceptability of surface imperfections, surface finish is measured in the direction that yields the highest deviation in surface profile.

8.3 POROSITY

Refer to Appendix A for porosity procedure and requirements.

8.4 UNUSED FINGERS

All unused (electrically unconnected) fingers must be on the final PWB. The exceptions are those fingers identified for removal on the MD drawing by a note identifying specific finger reference designators or as shown on the etch view of the MD drawing.

8.5 ADHESION

When tested in accordance with the requirements of IPC-TM-650, there shall be no evidence of plating removal except at the solder-gold butt line.

8.6 LENGTH

The minimum gold plating area and the critical contact area for each finger configuration are defined in text under subhead 8.11.3. Copper exposed at the butt line (the solder-gold or soldermask-gold boundary) shall measure no more than 0.030 inch (0.76 mm). See Figure 21.

8.7 WIDTH

The width of each plated finger shall have tolerances of ±0.010 inch (±0.25 mm) as inspected and measured for edge definition in accordance with the text under subhead 2.2.3 of IPC-TM-650. All standard fingers shall have a width of 0.080 inch (2.03 mm). All nonstandard fingers shall be as specified on the MD drawing or in EL-ENPCB-01 *PC Board Engineering Handbook— Standard Circuit and Finger Detail.*

8.8 SPACING

Finger-to-finger centerline tolerances shall be ±0.010 inch (±0.25 mm). Refer to EL-ENPCB-01 *PC Board Engineering Handbook— Standard Circuit and Finger Detail.* Also refer to Table 9, Spacing.

8.9 BEVEL

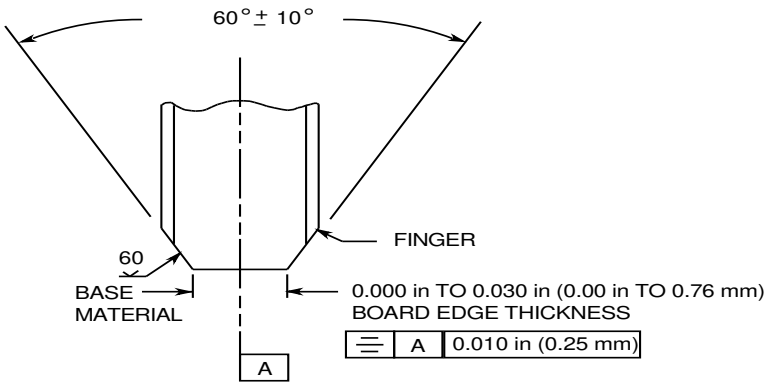
The outer (lower) end of each finger shall be beveled along its edge and on both sides.

a. The beveled surfaces meeting at an angle of 60° ±10°.

b. A board edge thickness of 0.000 inch to 0.030 inch (0.00 mm to 0.76 mm) to be symmetrical to the board centerline within 0.010 inch (0.25 mm).

c. A beveled machined surface finish not to exceed 0.00006 inch (0.0015 mm) arithmetic average (see text under subhead 8.2).

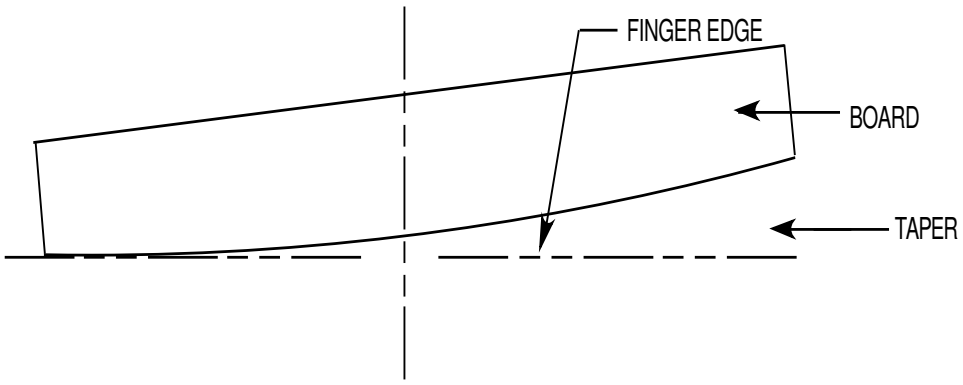
Figure 17: Bevel—Finger Edge



8.10 HEXBOARD EDGE TAPER

The finger edge(s) of each hexboard shall be tapered from the center, with the two tapered surfaces flat and perpendicular to the board plane. See Figure 20.

Figure 18: Edge Taper



When one tapered surface is set on a flat measuring plate and the board is perpendicular to the plate, the distance between the other tapered surface and the plate shall be 0.070 inch to 0.160 inch (1.78 mm to 4.06 mm) at the corner of the board.

8.11 OTHER FINGER CHARACTERISTICS

Other finger characteristics include breaks, flaking, wrinkling, peeling, dents, discoloration, inclusions, nicks, nodules, pinholes, pits, scratches, and voids.

For defect analysis, the total area of unused gold-plated contact fingers and pads shall be considered *noncritical*.

8.11.1 Breaks, Flaking, Peeling, and Wrinkling

There shall be no breaks, flaking, peeling, or wrinkling under any circumstances.

8.11.2 Discoloration

Discolorations that are permanently removable by assembly-cleaning operations are acceptable. Since different assembly sites choose different solvents from the list below, the PWB manufacturer must ensure that any discoloration is permanently removed by all of the following solvents.

a. Plain tap water

b. Water and saponifier

c. Isopropyl alcohol

d. Fluorinated solvents, such as Freon TMS

Discoloration must be removed by each solvent separately—no combinations or mixtures are allowed.

8.11.3 Dents, Inclusions, Nicks, Nodules, Pinholes, Pits, Scratches, and Voids

Dents, inclusions, nicks, nodules, pits, and scratches in the copper and nickel plate are acceptable under the following circumstances.

For defect analysis, the total area of unused gold-plated contact fingers and pads shall be considered *noncritical*.

a. Nickel and gold-plating thickness minimums are met.

b. Surface finish meets requirements under subhead 8.2.

Dents, inclusions, nicks, nodules, pinholes, pits, scratches and voids in gold-plating are acceptable under the following circumstances.

a. Nicks, pits, and scratches do not expose any nickel or copper.

b. The maximum length of each dent, inclusion, nick, nodule, pinhole, pit, scratch, or void does not exceed the following.

   1. 0.010 inch (0.25 mm) inside the critical contact area.

   2. 0.020 inch (0.51 mm) for any two of these imperfections, or 0.040 inch (1.02 mm) for any one of these imperfections located outside the critical contact area.

c. Surface finish meets requirements under subhead 8.2.

d. Nodules do not cause fingers to exceed their overall thickness and width tolerances.

e. The number of dents, nicks, pits, scratches, and voids per 18-finger group does not exceed the following on each side of the PWB.

- Inside the critical contact area:

  1. No more than one defect per finger
     AND
  2. No more than three fingers with defects

- Outside the critical contact area:

  3. No more than two defects per finger
     AND
  4. No more than six fingers with defects

f. The number of dents, nicks, pits, scratches, and voids *for PWBs with nonstandard finger groupings*, the maximum quantity of fingers with defects on each side of the PWB shall be determined by using the following percentages.

- Inside the critical contact area:

  1. No more than one defect per finger
     AND
  2. No more than 16.7% for fingers with defects (3/18 = 16.7%)

- Outside the critical contact area:

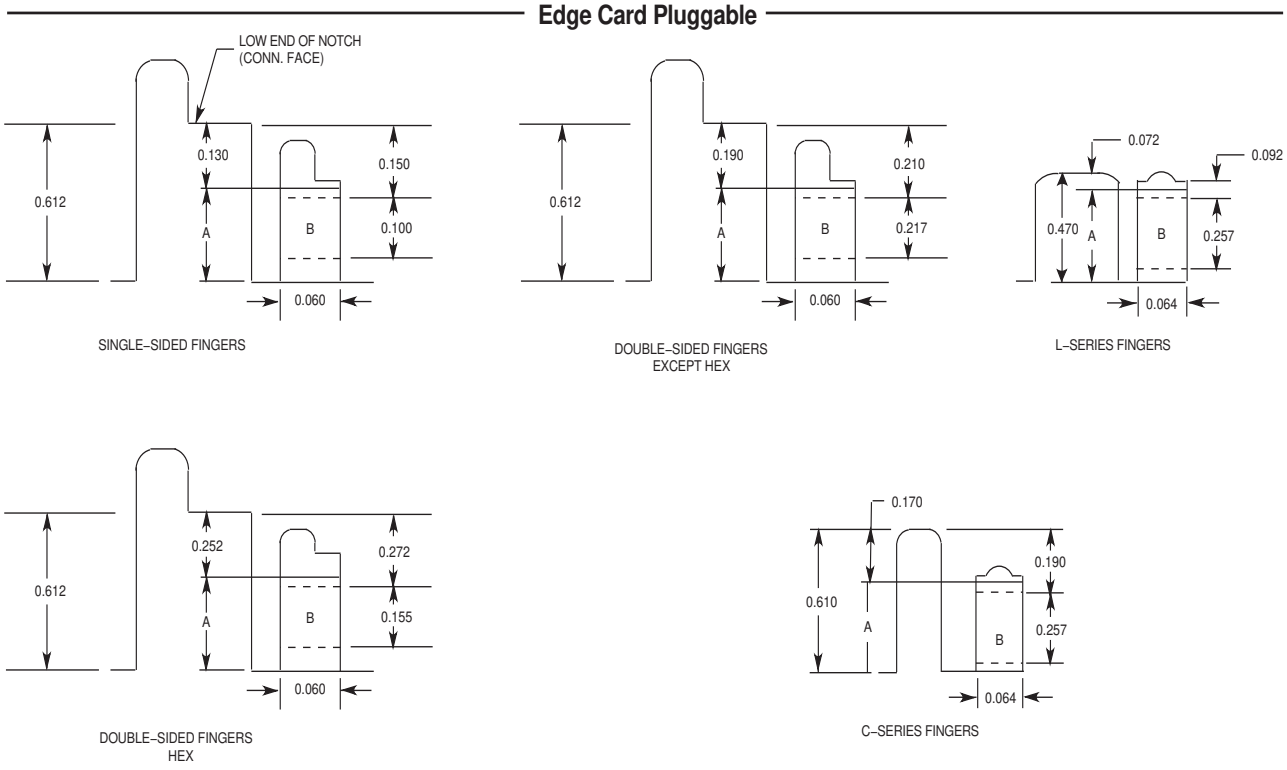
  3. No more than two defects per finger
     AND
  4. No more than 33% for fingers with defects (6/18 = 33%)

g. For inspection purposes, the following dimensions shall be used. These are shown in Figure 21.

1. For single-sided fingers, the critical contact area begins 0.15 inch (3.81 mm) from the low end of the notch and continues for a distance of 0.10 inch (2.54 mm).
2. For double-sided fingers except hex, the critical contact area begins 0.21 inch (5.33 mm) from the low end of the notch and continues for a distance of 0.217 inch (5.51 mm).
3. For double-sided hex fingers, the critical contact area begins 0.272 inch (6.91 mm) from the low end of the notch and continues for a distance of 0.155 inch (3.94 mm).
4. For C-series fingers, the critical contact area begins 0.190 inch (4.83 mm) from the notch and continues for a distance of 0.257 inch (6.53 mm).
5. For L-series fingers, the critical contact area begins 0.092 inch (2.34 mm) from the notch and continues for a distance of 0.257 inch (6.53 mm).
6. For F (8800 series), and T (VAXBI™ hardware) series gold-plated connector pads, the critical contact area is the full feature size. See Figure 19.
7. For F (8800 series), and T (VAXBI™ hardware) series gold-plated power and ground tabs, the critical contact area is specified in D-MD-ELEN624-00-DBU, E-MD-ELEN625-00-0, and D-MD-ELEN626-00-DBU contained in EL-ENPCB-01, *PC Board Engineering Handbook—Standard Circuit and Finger Details.* Refer to Figure 19.

8. For F (8800 series), and T (VAXBI™ hardware) series backplane connector (nongold-plated) tabs, refer to text under subhead 12.2 Unique Backplane Requirements.

Figure 19: Minimum Gold-Plating Length (Dimension A) and Critical Contact Area (Dimension B)



DIMENSIONS:
A. MINIMUM GOLD–PLATING = 0.650 in
B. CRITICAL CONTACT AREA = 0.080 in X 0.080 in SQUARE PAD

F AND T (VAXBI) SERIES CONNECTORS AND PADS
FOR DETAILS REFERENCE D–MD–ELEN626–0–DBU
E–MD–ELEN625–0–DBU, D–MD–ELEN624–0–DBU

9 SOLDERMASK

Soldermask shall cover etches to prevent bridging during the module solder process.

Soldermask types, placement, thickness, cure, solvent/flux resistance, flammability, abrasion resistance, adhesion, soldering requirements, and other characteristics are specified in the following sections. These requirements apply for side 1 and side 2 when a mask is applied.

9.1 TYPES

All soldermasks (dry film, wet screen, and wet photoimageable, including VALU) shall meet the following requirements. A full soldermask will be on the outside surface of all PWBs as specified below. All dry film soldermasks applied as a sole means of coverage shall be applied with a vacuum lamination process.

9.2 PLACEMENT

Soldermask placement and spacing requirements are specified in the text under the following subheads.

9.2.1 Board Side

The following placements and masks are allowed.

a. All high-density boards (C) with nominal conductor widths and spacings of 0.015 inch (0.38 mm) must have full soldermask on side 2.

b. All high-density boards (D) with nominal conductor widths of 0.012 inch (0.30 mm) and nominal conductor spacing of 0.013 inch (0.33 mm) must have a full soldermask on side 2 as a minimum.

c. All backplane boards must have a full soldermask on both sides (unless otherwise specified).

d. All high-density (H2D) and very high-density boards (E, F, G) with nominal conductor widths of 0.008 inch (0.20 mm) or less, or nominal conductor spacing of 0.010 inch (0.25 mm) or less, must have a full soldermask on both sides 1 and 2.

e. Unless otherwise specified, standard density boards (A, B) with conductor widths and spacings of 0.020 inch (0.51 mm) do not require soldermask.

9.2.2 Spacing/Coverage/Thickness Requirements

Soldermask spacing requirements are as follows.

a. Wet screen soldermask shall extend over both sides of the conductor or pad to the base laminate.

b. Wet photoimageable soldermask coverage is as follows.

   1. Conductor-to-Conductor—All metal must be completely encapsulated with a minimum 0.001 inch (0.025 mm) foot to the base laminate.

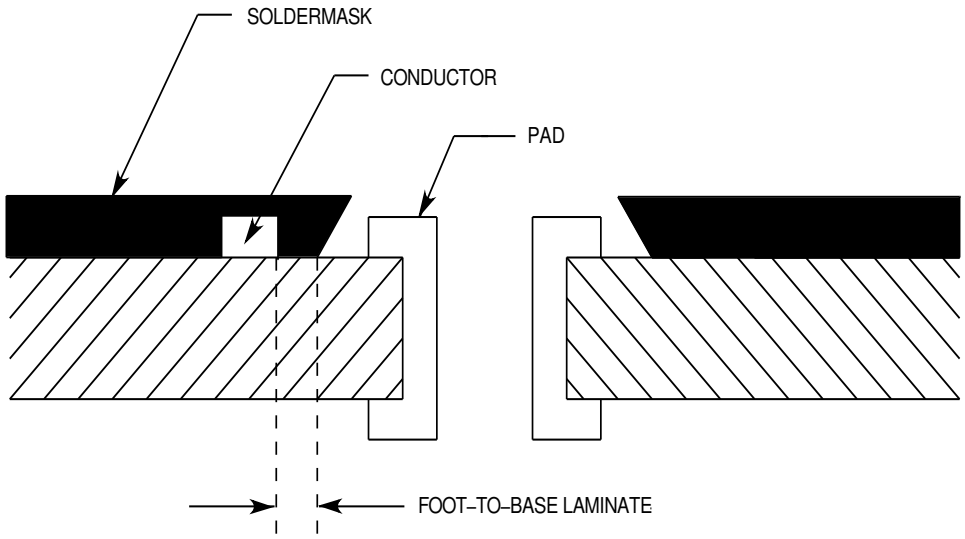
   2. Conductor-to-Pad—The conductor metal must be completely encapsulated with a minimum 0.001 inch (0.025 mm) foot to the base laminate.

3. Pad-to-Pad—Provided that pad-to-pad spacing meets or exceeds minimum soldermask spacing requirements, adjacent pads without conductors between them do not require soldermask to the base laminate. Adjacent pads with spacing below minimum require soldermask with a minimum 0.001 inch (0.025 mm) foot to the base laminate.

c. Dry film soldermask coverage is as follows.

1. Unless otherwise specified, dry film soldermask raw stock shall be 0.003 inch (0.076 mm) nominal, except as noted. Reflowed tin-lead PWB designs employing one ounce surface copper-foil thickness, soldermask over bare copper products, and backplanes that are not wave soldered (press-pin) may use 0.004 inch (0.102 mm) nominal thick dry film raw stock. For SMT products, see *DEC STD 176-4 Surface Mount Printed-Wiring Board Acceptance Criteria* subhead 9.
2. Conductor-to-Conductor—All metal must be completely encapsulated with a minimum 0.003 inch (0.076 mm) foot-to-base laminate. PWBs with vapor phase reflowed solder require 0.001 inch (0.025 mm) minimum foot-to-base laminate.
3. Conductor-to-Pad—The conductor metal must be completely encapsulated with a minimum 0.003 inch (0.076 mm) foot-to-base laminate. PWBs with vapor phase reflowed solder require 0.001 inch (0.025 mm) minimum foot-to-base laminate.
4. Pad-to-Pad—Provided that pad-to-pad spacing meets or exceeds minimum soldermask spacing requirements, adjacent pads without conductors between them do not require dry film soldermask-to-base laminate. Adjacent pads with spacing below minimum require dry film soldermask with a minimum 0.003 inch (0.076 mm) foot-to-base laminate.

Figure 20: Soldermask Foot-to-Base Laminate



d. On all PWBs, the soldermask shall not be closer than 0.002 inch (0.051 mm) to component holes and/or vias that are designed with soldermask clearance pads in the design data base.

e. Soldermask is not allowed on pads designated as test pads in the design data base.

f. Certain noncomponent holes/pads are selected by design to have a reduced soldermask clearance pad size equal to the finished hole size. This pad size is intended to cover (not *tent*) the pad with soldermask and thus prevent solder fill during wave solder. Since this clearance pad diameter is equal to the finished hole size, it is acceptable if there is soldermask inside the PTH hole wall only for these special noncomponent holes.

g. Full coverage of all conductive patterns is required with the exception of plated areas larger than 0.19 inch (4.8 mm) in width. Such areas require soldermask only on the edges for a maximum distance of 0.03 inch (0.76 mm) onto the area.

h. When soldermask thickness is in question, measurements shall be made by microsection, in accordance with IPC-TM-650. The minimum requirements when measured at the center of a masked conductor shall be in accordance with IPC-SM-840A *Qualification and Performance of Permanent Polymer Coatings (Soldermask) for Printed Boards*. See the text under heading 2 of this document for minimum magnification.

i. More than one application of soldermask is acceptable with the following exceptions.

- Mixing of different soldermask types and/or suppliers is not acceptable.
- The final soldermask thickness must not exceed UL recognized limits based on soldermask raw material, laminate grade, and laminate thickness. Refer to *DEC STD 176-02 Printed-Wiring Board Product Safety Criteria*.
- The final soldermask thickness on both sides of the PWB (where applicable) shall not cause the PWB to exceed the maximum allowable total board thickness.
- The final soldermask thickness shall not create any soldermask related problems in assembly.

9.3 CURE

The soldermask shall be fully cured and not exhibit tackiness, blistering, delamination, or color change when tested under controlled laboratory conditions as specified in IPC-TM-650.

Digital will use the evaporative rate analysis technique (Meseran) to assess the degree of soldermask cure. Refer to EL-MF601-00 *Test Method for Soldermask Cure*.

9.4 SOLVENT AND FLUX RESISTANCE

The soldermask shall not exhibit a degradation in surface characteristics, such as surface roughness, tackiness, blistering or color change, when tested under controlled laboratory conditions as specified in IPC-SM-840. (Not applicable to UV-curable soldermask.)

9.5 FLAMMABILITY

When tested in accordance with UL-94 *Test for Flammability,* soldermask applied to both sides of the PWB fabricators' minimum laminate thickness must achieve a flammability rating of 94V-1 or better.

9.6 ABRASION RESISTANCE

When tested in accordance of IPC-TM-650, the soldermask shall not be scratched by a pencil softer than an F hardness. (Such a pencil is available from local drafting supply houses.) Refer to *IPC-TM-650* subhead 2.4.27.2, Solder Mask Abrasion Pencil Method.

9.7 ADHESION

Adhesion conformance is to be determined using the following tape test described below. Conductor areas larger than 0.050 inch (1.27 mm) do not require tape testing.

1. Ensure that the board is clean and dry.
2. Obtain a strip of 0.50 inch (12.7 mm) adhesive tape equal to the length of the board and conforming to Federal Specification *A-A-113 Tape, Pressure-Sensitive Adhesive (Cellophane and Cellulose Acetate) (Formerly L-T-90),* Type II, Class B.
3. In an area where the conductor or line density is the highest, press the tape down tightly along the length of the board, ensuring that any air pockets are pressed out.
4. With a sharp pull approximately perpendicular to the pattern, rapidly remove the tape from the board.
5. If any peel condition exists from tape testing, the tested board should be run over the wave solder. If no soldermask defects, such as those specified in the text under subhead 9.8 are noted after the wave solder, the lot is acceptable.

9.8 SOLDER RESISTANCE

As determined below, the soldermask shall not adversely affect the solderability of the PWB.

a. After floating a fluxed 2 $\times$ 2 inches (51 $\times$ 51 mm) specimen in solder at 490°F (254°C) for 10 seconds, the soldermask shall completely resist the adherence of solder (webbing) and shall not peel.

b. The soldermask shall not exhibit separation from the base material of the board after processed through a component wave-soldering machine in accordance with Digital engineering specification A-SP-7665158-00-0, *Hollis TDC-16A Wave Soldering System: Process Control Requirements.*

c. Soldermask shall not allow tin/lead plate to squeeze up or squeeze out between conductors after processed through a component wave-soldering machine in accordance with Digital engineering specification A-SP-7665158-00-0.

9.9 OTHER SOLDERMASK CHARACTERISTICS

Other characteristics include blistering, voids, exposed conductors, and placement defects.

9.9.1 Blistering

Blistering is not acceptable with the following exception: minor blistering located in isolated areas and that do not bridge conductive patterns are allowed.

9.9.2 Voids

Except as specified in text under subhead 9.9.3, scratches, pinholes, and other forms of voids are acceptable provided the sides of the masked conductors are covered with soldermask.

9.9.3 Exposed Conductors and Pads

Scratches, pin holes and other forms of voids that occur on conductor edges and pad edges shall be allowed, provided that the distance to the nearest conductor or pad is greater than 0.015 inch (0.38 mm) or the nearest edge is completely covered. Nonadjacent exposed etches (metal-to-mask) are acceptable.

9.9.4 Exposed Copper

Processing defects such as scratches, pinholes, voids, and so forth, that result in exposed copper, are acceptable providing:

1. They are no larger than 0.125 inch (3.18 mm) in any direction on etch lines, ground planes, thieving, and etch nomenclature.
2. There is no exposed *adjacent* metal within 0.015 inch (0.381 mm).
3. Total exposed copper area is not to exceed 1% of surface area.
4. Exposed copper in vias resulting from breakdown of dry film *tents* or liquid photoimageable soldermask coverage is acceptable.

9.9.5 Placement Defects

Soldermask is acceptable in slots, notches, and cutouts if it does not reduce their dimensions below specification. Soldermask on fingers is acceptable, provided it does not extend into the minimum gold-plating area.

Soldermask on test pads is not acceptable.

10 MULTILAYER (ML) AND MULTISIGNAL-LAYER (MSL) PWBs

Unless otherwise specified, layer construction and layup detail drawings for 6, 8, and 10 layer multi-signal layer (MSL) boards with fingers are as follows.

C-MD-ELEN630-00-DBU	*Layer Construction, Board, 4-Layer*
D-MD-ELEN631-00-DBU	*Standard Layer Construction Detail, 6-Layer Board*
D-MD-ELEN632-00-DBU	*Standard Layer Construction Detail, 8-Layer Board*
D-MD-ELEN633-00-DBU	*Generic Layer Construction VAXBI™ Module Detail—10-Layer Board*
D-MD-ELEN635-00-DBU	*XMI Module Detail—10-Layer Module Construction*

NOTE

Detail drawings are contained in *EL-ENPCB-02 PC Board Engineering Handbook—Layer Construction Drawings*.

For MSL boards with fingers referencing these drawings in their documentation, overall board thickness and tolerances (measured over etch inclusive of all platings) and dielectric thickness and tolerances shall be as shown in the drawings, unless otherwise specified. Copper foil thicknesses and tolerances in the drawings are based on raw stock only.

Table 12: Copper Foil Thicknesses

Copper Foil Weight (oz/ft^2)	Copper Foil Thickness Raw Stock (inch)	Minimum Copper Foil Thickness (After PWB Processing) (inch)
1/2	0.0007 ± 0.0002	0.0003
1	0.0014 ± 0.0002	0.0010
2	0.0028 ± 0.0003	0.0022
3	0.0042 ± 0.0004	0.0036

For fingerless MSL boards, referring to the detail drawing listed under this subhead, the overall thickness (measured over etch inclusive of all platings) and dielectric thicknesses and tolerances shall be as shown in the detail drawings, unless otherwise specified. Copper foil thicknesses and tolerances in the detail drawings are based on raw stock only. The minimum copper foil thickness after PWB processing is given in Table 12 unless otherwise specified.

NOTE

The maximum overall PWB thickness inclusive of soldermask shall be the overall thickness measured over etch inclusive of all plating plus 0.004 inch (0.102 mm) per soldermasked side.

11 AUTOTHIEVING AND OTHER NONCONDUCTOR ETCH

This section describes the autothieving process and other nonconductor etch requirements.

11.1 AUTOTHIEVING

Autothieving is a process that adds current density sinks (nonfunctional plating areas) to a PWB during imaging. When autothieving is used, it shall meet the following criteria.

a. Standard autothieving (SA) shall not violate the minimum spacing requirements relating to PWB circuitry and pads. Transmission autothieving (TA) shall come no closer than what is required per the product data and will be documented on the mechanical drawing. If transmission autothieving is used, it will be documented on the mechanical drawing. The minimum spacing from autothieving pad edge to circuit edge is 0.025 inch (0.64 mm). For both types of autothieving, spacing violations between adjacent autothieving pads is acceptable. Date code and electrical test stamps are acceptable on both types of autothieving pads provided all permanence criteria is met.

b. The following items shall not be classified as defects on autothieving pads.

   1. Missing or extra pads
   2. Voids, nicks, scratches, pits, dents, and pin holes
   3. Poor fusing, nonwetting, or dewetting
   4. Soldermask registration, peel, missing, exposed autothieving pad to etch line or pad
   5. Copper or tin/lead thickness or peel
   6. Size of autothieving pad
   7. Exposed copper
   8. Burning roughness or wrong tin-lead alloy composition

11.2 NONCONDUCTOR ETCH

Nonconductor etch is electrically nonfunctional and serves various manufacturing and product identification needs, such as shearing crop marks, Digital logo, part number/layer numbering, product safety marking, and so on. Defects listed in 11.1 (b) are acceptable providing the intended function of the nonconductor etch (such as permanence or legibility) is not affected.

12 BACKPANEL BOARDS

This section describes backplane connector hole size and unique backplane requirements.

12.1 BACKPLANE CONNECTOR HOLE SIZES

This section describes press-pin, wave solder, and other backplane hole size requirements.

12.1.1 Press-Pin Backplane Primary Hole Size

For press-pin backplane boards using connectors with pins on 2.54 mm (0.100 in) centers, the connector pin primary drill hole size is 1.14 mm (0.045 in) minimum. The primary hole size is the diameter of the hole after drilling. It must be verified prior to plating.

For press-pin backplane boards, using connectors with pins on 2 mm (0.079 in) centers, the connector pin primary drill size is 0.85 mm (0.0335 in). The primary hole size is the diameter of the hole after drilling and shall be 0.81 mm to 0.86 mm (0.032 in to 0.034 in). The primary drilled hole must be verified prior to plating.

12.1.2 Press-Pin Backplane Finished Hole Size

For press-pin backplane boards, using connectors with pins on 2.54 mm (0.100 inch) centers, the connector pin finished hole size shall be 1.04 mm (0.041 inch) +0.051/-0.076 mm (+0.002/-0.003 in).

For press-pin backplane boards, using connectors with pins on 2 mm (0.079 inch) centers, the connector pin finished hole size shall be 0.65 mm to 0.80 mm (0.026 in to 0.031 in).

12.1.3 Wave Solder Backplane Hole Sizes

For wave solder backplane boards, the connector pin finished hole size shall be 0.042 inch (1.067 mm) ±0.005 inch (±0.127 mm).

12.1.4 Other Backplane Hole Sizes

Unless otherwise specified, finished hole sizes for nonconnector related holes shall be as stated in the text under subhead 5.2.1 Plated-Hole Diameters.

12.2 UNIQUE BACKPLANE REQUIREMENTS

The following criteria relates to unique backplanes containing solder connector contact pads.

12.2.1 Backplanes with Solder Connector Contact Pads

a. Critical contact area

   The critical contact area is identified by A and F in Figure 21.

   When determining critical contact area for power pads, a line from adjacent signal pads can be used to project a reference point from which the critical area can be determined. This method can be used to determine critical contact area for any power pad configuration on backplanes with solder connector contact pads.

   Dents, inclusions, nicks, nodules, pinholes, pits, scratches, and exposed copper are acceptable under the circumstances listed in Table 13.

b. Solder thickness—Solder connector contact pads

   Solder thickness for the connector contact footprint pads (areas A, B, and F in Figure 21) shall be a minimum of 0.0003 inch (0.0076 mm) and shall not exceed 0.0015 inch (0.0381 mm), as measured at the crest.

c. Solder thickness—Other areas

Minimum solder thickness in areas not associated with the solder connector contact pads shall be as stated in the text under subhead 6.5.

d. Electrical test

Electrical contact for shorts or opens test may be made to the surface pads in the critical area with the following constraints.

The supplier must get Digital approval of the test fixture and probes. Any changes to the fixturing or probes require Digital approval.

1. Probe contact material must not be gold.
2. Contact pressure will be less than 0.07 oz/sq. mil (3.1 kg/mm^2)

Figure 21: Solder Backplane Critical Contact Area

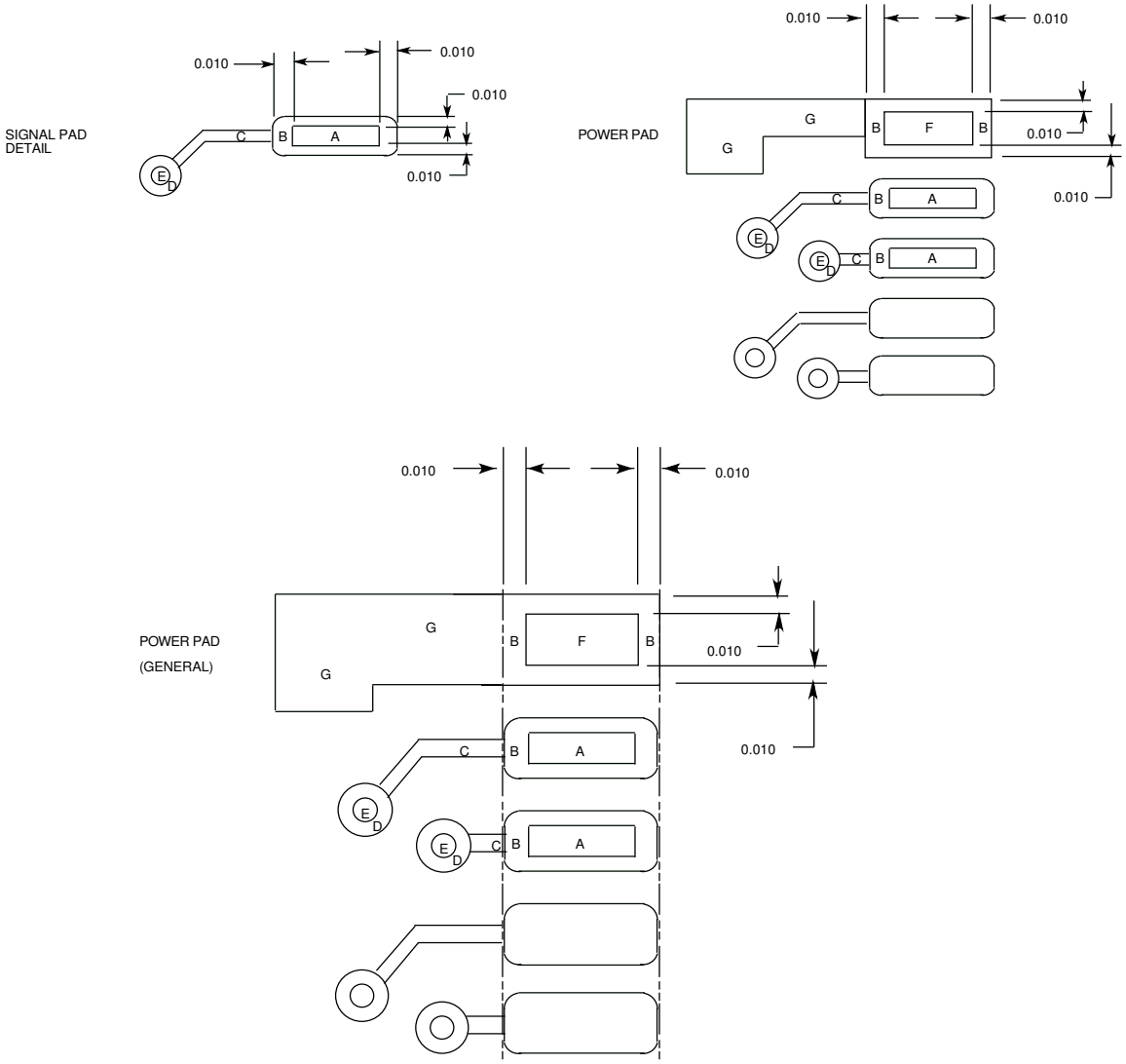


Table 13: Defect Criteria—F and T Backplane Connector Solder Pads

	Contact Area						
DEFECTS	A	B	C	D	E	F	G
Exposed copper	rej*	OK	OK	OK	rej*	rej*	OK
Dewetting ***	rej*	OK	OK	OK	OK	rej*	OK
Surface damage	**	OK	OK	OK	OK	**	OK

* Can be reworked with approved rework process. See *DEC STD 176-1 Printed-Wiring Board Repair Criteria*.
** According to text in DEC STD 176-0 subhead 8.11.3.
*** Dewetting is acceptable providing the minimum thickness of tin/lead (Sn/Pb) is met.

13 ELECTRICAL CHARACTERISTICS

Interconnection resistance, continuity, and additional multilayer requirements are specified in the following subheads.

13.1 CONDUCTOR INTERCONNECTION RESISTANCE

When measured in accordance of IPC-TM-650, the interconnection resistance from any terminal area (pad or finger) to any other terminal area on the same side of the board shall not be greater than 0.001 ohm for each 0.125 inch (3.18 mm) of conductor length.

NOTE

This paragraph requires use of the IPC-TM-650 test pattern.

13.2 CONTINUITY

As a minimum, all multilayer PWBs, backplanes, and 15/15 density boards and higher technologies shall require electrical testing. There shall be no shorts between adjacent conductors or between adjacent networks of interconnected conductors as defined in the design data base. There shall be no opens between any conductors or networks defined as connected in the design data base.

13.3 ADDITIONAL ML AND MSL REQUIREMENTS

Special HIPOT tests, insulation resistance, current capacity, impedance, and capacitance criteria are specified below for ML and MSL boards.

13.3.1 Dielectric Withstanding Voltage (HIPOT)

All MSL boards 8-layers and greater shall be tested in accordance with subhead 2.5.7 of IPC-TM-650 Class A requirements with the following exceptions:

a. The test specimen is the actual PWB.

b. The test voltage will be applied across all power and ground networks of the PWB specified by design documentation.

c. The test leads will not be soldered to the PWB.

d. Voltage will be raised from 0 to 1,000 Vdc value at an approximate rate of 200 volts per second.

e. Maximum voltage will be maintained for 10 seconds minimum.

f. Upon completion of test, voltage will be reduced to 0 by gradual reduction at an approximate rate of 200 volts per second.

g. All HIPOT tested PWBs shall be marked with an *Hp* stamp.

During the time of test, there shall be no audible or visual sparkover or breakdown by internal or external conductive patterns. In addition, the leakage current flow at maximum voltage shall not exceed 10 microamperes.

When automated HIPOT testing is used, the test requirements of items (a) through (e) must be met. In addition, while reducing the voltage from 1000 Vdc to 0, the automated tester must provide current limiting to a maximum of 10 amperes for a duration of 1 second maximum.

13.3.2 Insulation Resistance

When measured in accordance with IPC-TM-650, and 100 Vdc applied, a resistance greater than 100 megohms shall be recorded between the following.

a. Any point on the power plane and any point on the ground plane

b. The ground plane and plated-through holes not connected to the ground plane

c. The power plane and plated-through holes not connected to the power plane

13.3.3 Current Capacity

To Be Determined

13.3.4 Impedance

When required, impedance shall be determined to be within product specification as measured with a calibrated time domain reflectometer (TDR). Equipment, procedures, and probe points must be approved by Digital. The accuracy of the test reading must be confirmed between the PWB supplier and Digital.

Generally, impedance is measured with a coupon that is designed within the circuit area. However, for designs with insufficient routing area for an on-circuit coupon, a test coupon must be placed on the manufacturing panel external to the circuit. This coupon must be located greater than or equal to 0.250 inch (6.35 mm) and less than or equal to 1.000 inch (25.40 mm) from the circuit edge. Where there is more than one circuit per manufacturing panel, only one coupon is required, and it shall be positioned to be representative of the processing received by each circuit on the panel.

All impedance controlled circuits must be serialized. A coupon placed external to the circuit must be serialized and traceable to that circuit. When a single coupon is used to represent processing multiple circuits on a manufacturing panel, all circuits on the panel, as well as the coupon, will have the same serial number. When specified in product engineering documentation, impedance measurements traceable to each circuit (or coupon), as well as the physical coupon (where applicable), must be supplied as specified. Unless otherwise specified, suppliers that can demonstrate conformance to impedance requirements by means of process capability and statistical process control may request approval from Digital to employ reduced impedance testing on a statistical sampling basis.

13.3.5 Capacitance

When required, capacitance shall be determined to be within product specification as measured with a calibrated capacitance meter. Equipment, procedures, and probe points must be approved by Digital. The accuracy of the test reading must be confirmed between the PWB supplier and Digital.

Generally, capacitance is measured with a coupon that is designed within the circuit area. However, for designs with insufficient routing area for an on-circuit coupon, a test coupon must be placed on the manufacturing panel external to the circuit. This coupon must be located greater than or equal to 0.250 inch (6.35 mm) and less than or equal to 1.000 inch (25.40 mm) from the circuit edge. Where there is more than one circuit per manufacturing panel, only one coupon is required, and it shall be positioned to be representative of the processing received by each circuit on the panel.

All capacitance-controlled circuits must be serialized. A coupon placed external to the circuit must be serialized and traceable to that circuit. When a single coupon is used to represent processing multiple circuits on a manufacturing panel, all circuits on the panel as well as the coupon will have the same serial number. When specified in product engineering documentation, capacitance measurements traceable to each circuit (or coupon), as well as the physical coupon (where applicable), must be supplied as specified. Unless otherwise specified, suppliers that can demonstrate conformance to capacitance requirements by means of process capability and statistical process control may request approval from Digital to employ reduced capacitance testing on a statistical sampling basis.

13.3.6 Thermal Stress—ML and MSL PWBs

Thermal Stress Testing per text under subhead 7.5 shall be performed as part of PTH/laminate quality evaluation. Refer to text under subhead 5.2.3 to interpret test results.

14 ALLOWABLE REPAIRS

Digital and supplier personnel not of Digital may perform repairs as specified in *DEC STD 176-1 Printed-Wiring Board Repair Criteria.* After repair, the board must meet all physical, electrical, cosmetic, workmanship, and cleanliness requirements specified in this standard.

15 PRODUCT SAFETY

All Product Safety and UL requirements are specified in DEC STD 176-2.

16 PACKAGING

In addition to good commercial practice in packaging, marking, shipping, and storing the following packaging requirements shall be met.

a. Prior to packaging, all PWBs shall be clean and dry.

b. All packaging must be suitable for the prevention of static buildup, scratching, bending, fracturing and puncturing, impact, compression, moisture, corrosion, and chemical damage.

c. In any one package, each board must be separated from an adjacent board by suitable packaging or wrapping material.

d. Any paper or cardboard used for wrapping or separating individual boards shall be chemically neutral PH 6.5 to PH 7.5. In addition, the maximum amount of dissociable sulfur shall be 0.0008 percent by weight.

e. Heat may be used to seal plastic bags or wrappings, provided that venting is provided for entrapped gases.

f. The number of boards per package shall be suitable for easy handling and stacking in a stockroom system—normally no more than 30 pounds per package for manual operations.

17 QUALITY ASSURANCE TESTS

Unless otherwise specified, the following quality assurance tests in IPC-TM-650 are applicable for the purposes of this standard.

NOTE

Some of the following tests may require the use of special IPC-TM-650 test patterns.

Table 14: IPC-TM-650 Quality Assurance Tests

Subhead	Title
	Dimensional Tests
2.2.1	Annular Ring Measurement
2.2.2	Conductor Width and Spacing
2.2.3	Conductor Edge Definition
2.2.6	Hole Size Measurement, Drilled
2.2.7	Hole Size Measurement, Plated
2.2.8	Location of Holes
2.2.9	Overhang and Undercut Measurement
2.2.10	Registration of Conductors
2.2.11	Registration, Terminal Pads (Layer-to-Layer)
2.2.13	Thickness, Plating in Holes
2.2.13.1	Thickness, Plating in Holes, Micro-ohms Method
	Chemical Tests
2.3.9	Flammability of Prepreg Materials
2.3.23	Soldermask Cure (Permanency), Thermally Cured Masks
2.3.24	Porosity of Gold Plating (Chemical Method)
2.3.25	Detection of Ionizable Surface Contamination (Static Method)
2.3.26	Detection of Ionizable Surface Contamination (Dynamic Method)
2.3.27	Resistance to Fluxes (Soldermask)
2.3.28	Resistance to Solvents (Soldermask)
	Mechanical Tests
2.4.1	Adhesion, Plating
2.4.1.1	Adhesion, Marking Paints and Inks
2.4.12	Solderability, Edge Dip Method
2.4.14	Solderability of Metallic Surfaces
2.4.14.1	Solderability, Wave Solder Method
2.4.21	Terminal Pull Strength, Rigid Printed-Wiring Board
2.4.22	Warp and Twist

* Requires use of IPC-TM-650 test pattern, unless otherwise specified.

Table 14 (Cont.): IPC-TM-650 Quality Assurance Tests

Subhead	Title
	Mechanical Tests
2.4.27.2	Soldermask Abrasion (Pencil Method)
2.4.28 *	Adhesion, Soldermask
	Electrical Tests
2.5.3	Current Breakdown, Plated-Through Holes
2.5.7	Dielectric Withstanding Voltage, Multilayer Printed-Wiring
2.5.10 *	Insulation Resistance, Multilayer Printed-Wiring (Between Layers)
2.5.11 *	Insulation Resistance, Multilayer Printed-Wiring (Within a Layer)
2.5.12 *	Interconnection Resistance, Multilayer Printed-Wiring
2.5.16	Shorts, Internal on Multilayer Printed-Wiring

* Requires use of IPC-TM-650 test pattern, unless otherwise specified.

APPENDIX A POROSITY PROCEDURE

A.1 CONTACT POROSITY

This section shows how to determine the integrity of the metallic gold plating on the areas that function as electrical contact surfaces. This porosity test process cleans, depolarizes, and activates the substrate metal exposed in the pores and attacks them sufficiently to cause reaction products to fill the pores up to the surface of the plating.

A.1.1 EQUIPMENT

Following is the test equipment required to determine the integrity of the plating.

a. Test chamber:

   The test chamber may be any convenient size glass vessel having a gas-tight lid. A 250 mm inside diameter, glass desiccator with a gas tight lid is recommended. A Fisher Scientific Company Series 08-595 or equivalent works well.

   The ratio of the test chamber volume in cubic centimeters to the porosity generating solution (nitric acid, HNO_3) surface area in square centimeters shall not exceed 25/1 (volume in cubic inches to square inches shall not exceed 10/1).

b. Specimen holders:

   Glass, polytetrafluoroethylene, or other inert material may be used to hold the parts under test in the upper part of the desiccator.

c. Magnifiers and illuminators:

   A stereomicroscope with a 10X magnification shall be used to count pores. In addition, a movable source of illumination capable of giving oblique lighting on the specimen surface shall be used.

d. Reagents:

   1. Reagent grade concentrated nitric acid (70 ± 1% HNO_3, specific gravity 1.415 to 1.420)
   2. Reagent grade 1,1,1-trichloroethane, or other suitable cleaning solvent

e. Handling equipment:

   Tweezers, microscope lens tissue or clean, soft cotton gloves shall be used.

f. Oven, air circulating:

   The oven shall be capable of maintaining 125 ± 5°C (257 ± 9°F).

g. Ultrasonic cleaning apparatus

A.1.2 REQUIREMENT

The porosity test's requirement is to reveal the individual pore indications and reaction products that fill the pores to the surface of the plating. Pore indications (corrosion products) shall be evaluated at 10X magnification on the specified contact areas. The acceptable level of pore indications on the specified contact areas shall meet the criteria given in the text under subhead A.1.4.

A.1.3 METHOD

This section describes the method used to determine contact porosity.

A.1.3.1 Cleaning and Handling Specimens

Handle specimens as little as possible and only with tweezers, microscope lens tissue, or soft cotton gloves.

Prior to the test, thoroughly clean the samples ultrasonically with fresh reagent-grade 1,1,1-trichloroethane, or other suitable cleaning solvent and air dry with filtered air. Inspect the cleaned part at 10X magnification for evidence of particulate matter on the surface. If any particulate remains, clean again with solvent and use a clean soft brush to remove the particulate prior to starting the porosity test.

NOTE

Do not touch samples with bare fingers after cleaning.

It is important to rinse the desiccator thoroughly and dry it completely before adding the acid. If the old acid is discarded and residual acid droplets remain in the desiccator when the room humidity is greater than 60% relative humidity (RH), sufficient moisture can be picked up to change the vapor pressure equilibrium.

CAUTION

The cleaned samples must be thoroughly dry before testing to ensure that residual moisture will not accelerate corrosion at the pore sites.

A.1.3.2 Equipment Preparation

Prepare equipment as follows.

a. Place the desiccator in a ventilated fume hood.

b. Do not grease the surface of the acid desiccator or cover.

c. Using site-specific laboratory safety precautions, add the HNO_3 to the bottom of the clean dry desiccator. Be careful not to splash any acid. Immediately seal the cover. Wipe droplets off the sides with a clean, dry, lint-free towel.

NOTE

The ambient relative humidity shall be no greater than 60% during the addition of HNO_3.

d. All equipment and reagents shall be in a controlled environment of 23 ± 3°C (73 ± 5°F) and a maximum of 60% RH.

e. Allow 30 ± 5 minutes for equilibrium to be established.

A.1.3.3 Nitric Acid Vapor Test

The nitric acid vapor test follows.

a. The test temperature shall be 23 ± 3°C (73 ± 5°F) and the relative humidity in the immediate vicinity of the test chamber shall be no greater than 60%.

NOTE

If the relative humidity is greater than 60%, do not run the test.

b. Carefully remove the desiccator cover.

c. Immediately place the specimen holders with the samples into the desiccator and reseal the cover to prevent an excessive loss of vapors that would disrupt the equilibrium previously established.

CAUTION

Sample Placement: Specimens shall not be closer than 25 mm (1 in) from the wall and 75 mm (3 in) from the solution surface. Specimens shall be at least 13 mm (0.5 in) from any other surface being evaluated.

d. The test duration is dependent on the gold-plating thickness. The exposure time required is as specified in the following table.

Gold layer thickness	HNO_3 Sample exposure time
0.76 to 1.27 micrometers (30 to 50 microinches)	30 ± 5 minutes
Greater than 1.27 micrometers (Greater than 50 microinches)	60 ± 10 minutes

e. Remove the samples at the end of the test exposure time specified in (d) and transfer the samples immediately to an oven at 125°C (257°F) for 30 minutes to dry the moist corrosion product.

NOTE

Unless otherwise specified, the HNO_3 solution may be reused within an 8 hour period, provided the desiccator has been maintained at the temperature and humidity specified in subhead A.1.3.2, item d. Do not reuse acid if condensation appears on the inside of the desiccator or if a yellow-brown vapor is present in the desiccator.

f. Discard the HNO_3 solution according to site-specific waste treatment procedures.

A.1.3.4 Corrosion Product Examination

After drying, the gold-plated contacts shall be inspected for corrosion spots at 10X magnification, using collimated incandescent illumination at an oblique angle below 15°.

The presence of pores will be delineated by the protruding corrosion products from their sites. These corrosion products may be transparent or pale-blue in color.

Each reaction product spot indicates a pore in the plating.

A.1.3.5 Corrosion Product Report and Evaluation Data Requirements

The quantity and corresponding size of the pores or corrosion products on the required contact surface area plated with gold shall be obtained under 10X magnification by counting pore sizes and pore-corrosion product areas.

NOTE

Pore sizes less than 0.05 mm (0.002 in) are not resolvable at 10X. Therefore, they are not counted.

Corrosion of unplated contact edges are not considered porosity.

Stains are not considered porosity.

Loose contamination that can easily be removed by a gentle air blowing are not be considered corrosion products.

A.1.4 DATA INTERPRETATION

On a per contact basis:

a. The combined area of pore size and pore-corrosion products shall not cover the contact surface area more than:
   - i 30% for <0.13 mm (0.005 in) diameter
   - ii 20% for 0.13 to 0.38 mm (0.005 to 0.015 in) diameter
   - iii 0% for >0.38 mm (0.015 inch) diameter

b. If a combination of a(i) and a(ii) are visible, then the combined pore size and pore-corrosion product area shall cover no more than 20% of the contact surface area.

c. The largest pore combined size and pore-corrosion product area visible at 10X magnification shall not be greater than 0.38 mm (0.015 in) diameter. If it is an irregular shape, the greatest dimension shall not exceed 0.38 mm (0.015 in).

d. Pore corrosion product resulting from scratches, nicks, dents, or other mechanical abrasions should not be included in the data interpretation.

APPENDIX B CALCULATION AND CONVERSION OF TRUE POSITION TOLERANCE

B.1 TO CONVERT GEOMETRIC LOCATION (±) TOLERANCE (GLT) TO TRUE POSITION DIAMETER (TPD):

$$TPD = 2\sqrt{(+Tolerance)^2 + (-Tolerance)^2}$$

Example: For GLT ±0.003 inch

$$TPD = 2\sqrt{(0.003)^2 + (0.003)^2} = 0.0085\ inch$$

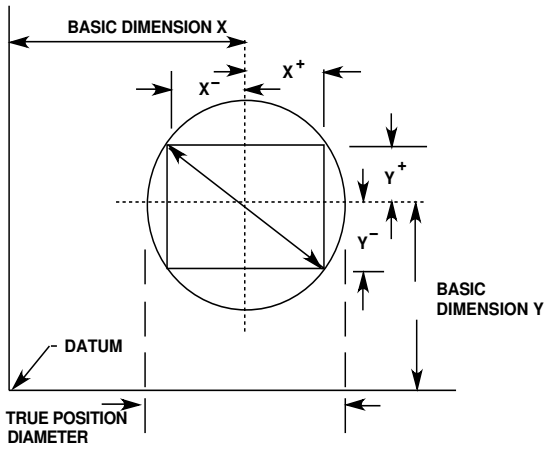
B.2 TO CONVERT FROM TRUE POSITION DIAMETER TO GEOMETRIC LOCATION (±) TOLERANCE:

$$GLT = 0.3535 \times TruePositionDiameter$$

Example: For TPD, 0.0057:

$$GLT = 0.0057\ inch \times 0.3535 = \pm 0.002\ inch$$

Figure 22: Position Tolerance



NOTE

Further information on true position tolerancing can be found in *ANSI Y14.5M-1982 (R 1988) Dimensioning and Tolerancing*.

APPENDIX C WARPAGE MEASUREMENT PROCEDURE

C.1 SCOPE

This procedure provides a standardized methodology for the measurement of warpage (bow and twist) of finished rigid PWBs, furnished in panel (multiple PWBs) or single PWB assembly board forms.

C.2 APPLICABILITY

This procedure applies to PWBs of all technologies specified in EL-SM176-00, *Printed-Wiring Board Manual*.

C.3 DEFINITIONS

Consistent with *DEC STD 016-0 Printed-Wiring Board and Module Manufacturing Terminology* and *IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits* PWB terms and definitions, the term *warpage* should be avoided. The terms *bow* and *twist* shall be used to describe the specific deviations from true flatness implied by the less specific term *warpage*.

C.3.1 BOW

Bow is a planar deviation from flatness that can be characterized by a roughly cylindrical, or spherical curvature, when a rectangular PWB is placed unrestricted on a true flat surface. Refer to Figures 23 and 24. In addition to the curvature, all four corners of the PWB must touch the flat surface (therefore, all corners are in the same plane) in order to be completely characterized as bow.

C.3.2 TWIST

Twist is a nonplanar deviation from flatness that can be characterized in a similar fashion as bow except that when a rectangular PWB is placed unrestrained on a true flat surface, one (or two) of the four corners of the PWB will not touch the flat surface (therefore all four corners are not in the same plane) when twist is present.

C.3.3 BOW AND TWIST

In many instances bow and twist may be present when a PWB is placed unrestrained on a true flat surface. The methodology described in this procedure must be used to identify the predominant source of the deviation from true flatness (bow or twist) for the purposes of finished PWB acceptance.

C.4 LIMITATIONS AND PRECAUTIONS

The methodology described in this procedure determines the maximum measured deviation from flatness along the length (bow), width (bow), or diagonal (twist) of a rectangular PWB board placed unrestrained on a true flat surface. The bow or twist is expressed as the ratio of the maximum measured deviation and the total distance (length, width, or diagonal) along the PWB edge (from corner to corner in the same plane) where the maximum deviation from flatness is present. The resulting factor (inch/inch or mm/mm) is an overall measure of bow or twist. The incremental deviations from flatness along the total length of the curvature exhibited by the PWB surface could be more, less, or equal to the computed factor resulting from this procedure.

As a precautionary note, many depanelization methods used to assist the Module Assembly process in reducing assembled modules to final outline dimensions (for example, *knock out* hole patterns, routed *dog ears*) will add to the overall bow or twist of the assembly board (Refer to Figure 1).

C.5 APPARATUS

The following apparatus is required to perform the measurement procedures described below.

a. Metrology grade granite surface plate

b. Metrology grade pin gauges

c. Linear measurement device of suitable accuracy

C.6 PROCEDURES

This section describes the procedures to measure bow or twist.

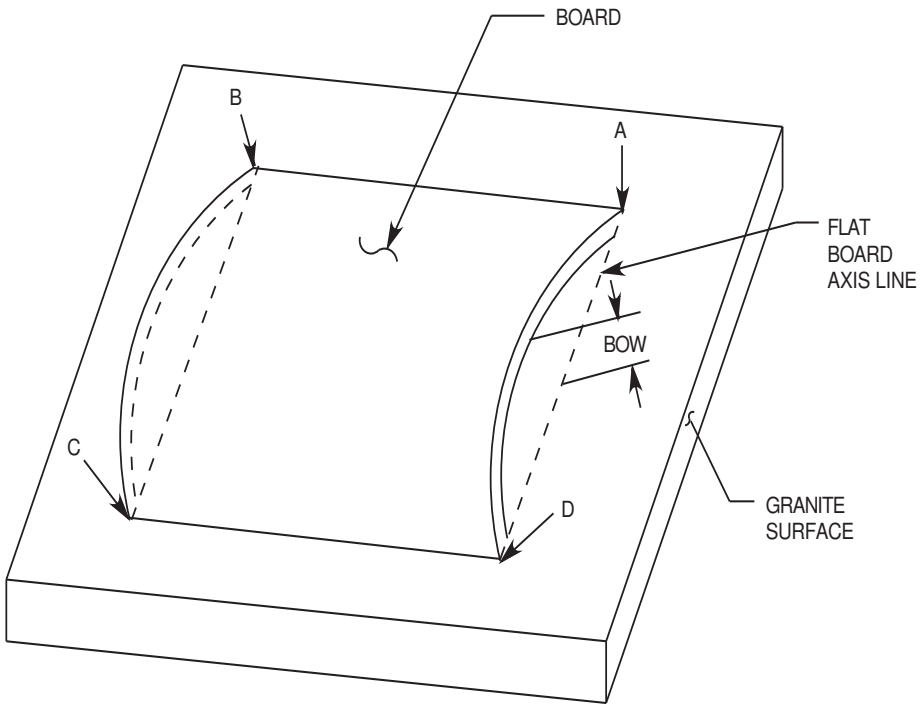
C.6.1 BOW

Place the PWB unrestrained on the granite surface plate such that the convex surface (bow) is facing upwards. If there is no twist present, all four corners will touch the granite surface without any pushing or coaxing. Refer to Figures 23 and Figure 24.

Generally, the region of maximum deviation from the granite surface plate can be visually detected. If this is not the case, for each of the four edges of the PWB identify the largest pin gauge that will fit in any gap between the board and the surface plate without lifting, pushing down on corners, or otherwise disturbing the position of the board.

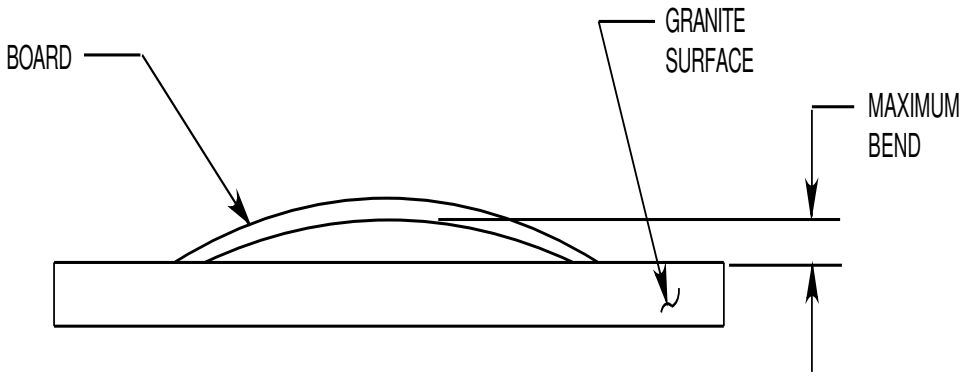
When identified, divide the diameter of the pin gauge representing the maximum deviation from the surface plate by the total length of the printed-wiring board edge associated with the maximum deviation. The resulting factor in units of inch-per-inch (mm-per-mm) is the bow of the PWB that must be compared to the allowable values specified in DEC STD 176-0, subhead 3.4, Table 3 for all nonsurface mount products or *DEC STD 176-4 Surface Mount Printed-Wiring Board Acceptance Criteria*, Table 2 for all surface mount products.

Figure 23: Bow (Top View)



NOTE: POINTS A, B, C, AND D ARE TOUCHING GRANITE SURFACE.

Figure 24: Bow (Side View)



C.6.2 TWIST

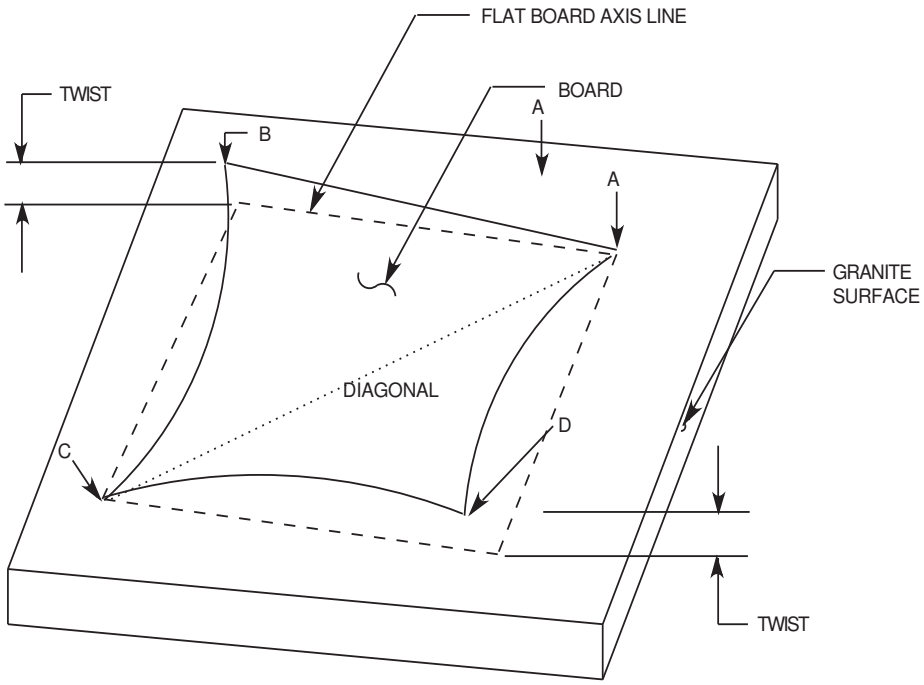
Twist results from a *fold* in the PWB axis along its longest dimension, usually the diagonal. When the twist axis is approximately along the diagonal of the PWB, and when placed unrestrained on the granite surface plate, two corners of the PWB will typically contact the surface plate. The opposite corners will rock back and forth but will not touch the surface plate unless force is applied to one corner. Refer to Figure 25. When the twist axis is significantly off the diagonal of the PWB, when placed unrestrained on the granite surface plate, typically three corners of the PWB will contact the surface plate without any added force.

C.6.2.1 TWIST AXIS ON THE DIAGONAL

Place the PWB unrestrained (no added force) on the granite surface plate such that the maximum deviation from the surface plate is obtained. This may involve placing the PWB on the surface plate with convex surface facing up or down. When the twist axis is approximately on the diagonal, two corners of the PWB will typically contact the surface plate without added force and two corners will not. Refer to Figures 25 and 26. Identify the largest pin gauge that will fit in the gap between each board corner and the surface plate without lifting or otherwise disturbing the position of the board.

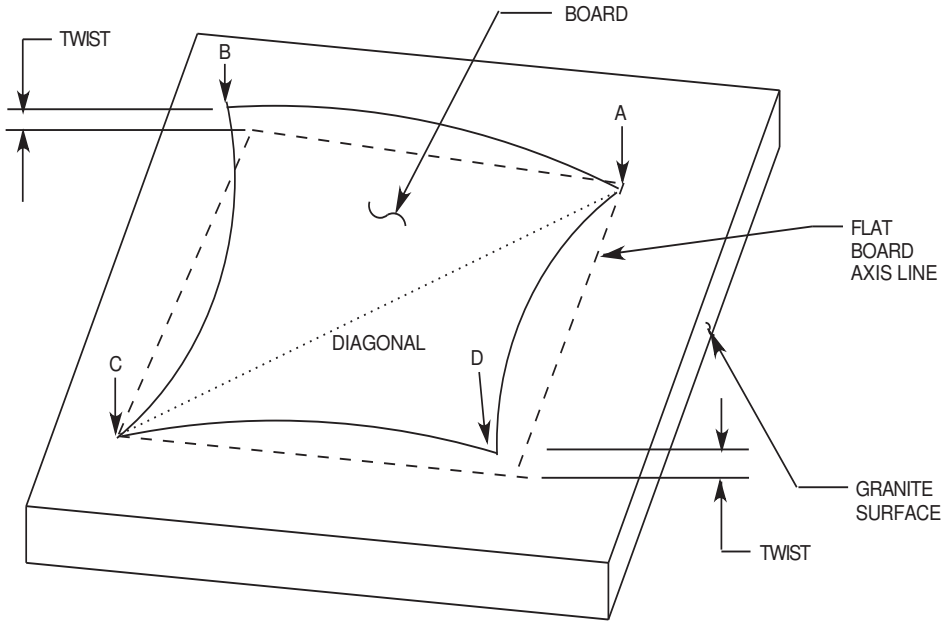
The twist factor is determined by dividing diameter of the pin gauge associated with the maximum deviation from the surface plate by the diagonal length of the PWB. The resulting factor in units of inch-per-inch (mm-per-mm) must be compared to the allowable values specified in DEC STD 176-0, Table 3, for all nonsurface mount products or DEC STD 176-4, Table 2 for all surface mount products.

Figure 25: Twist—Natural Resting Position (Concave) Without Added Force



NOTE: POINTS A AND C ARE TOUCHING GRANITE SURFACE.

Figure 26: Twist—Natural Resting Position (Convex) Without Added Force



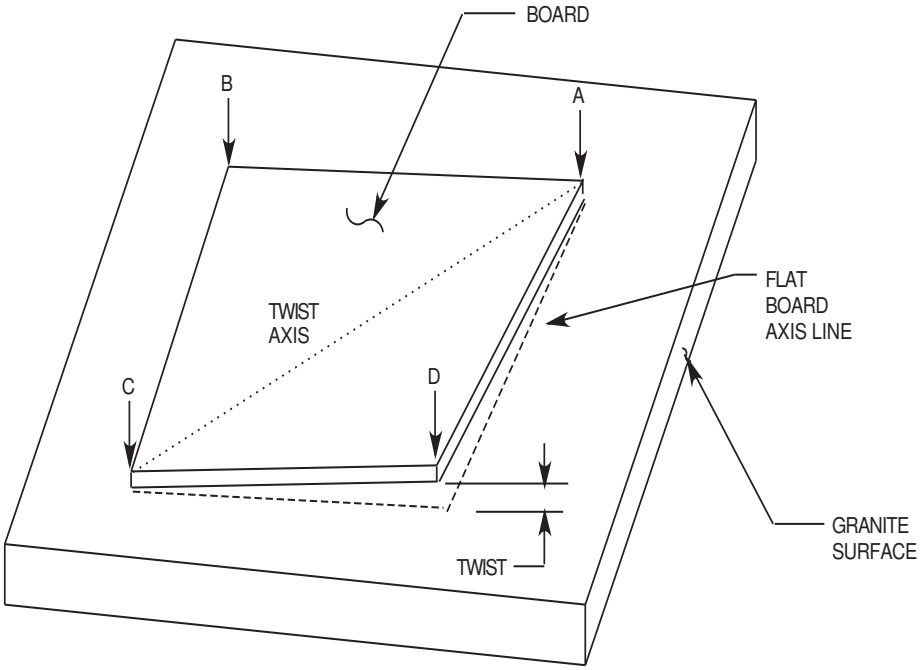
NOTE: POINTS A AND C ARE TOUCHING GRANITE SURFACE.

C.6.2.2 TWIST AXIS NOT ON THE DIAGONAL

Place the PWB unrestrained on the granite surface plate so that the maximum deviation from the surface plate is obtained. This placing may involve positioning the PWB on the surface plate with convex surface facing up or down. Refer to Figure 27. When the twist axis is significantly off the diagonal, three corners of the printed-wiring board will typically contact the surface plate without added force and one corner will not.

Identify the largest pin gauge that will fit in the gap between the board corner and the surface plate without lifting or otherwise disturbing the position of the board.

Figure 27: Twist—(Concave)



NOTE: POINTS A, B, AND C ARE TOUCHING GRANITE SURFACE.

In order to compute the twist factor, the actual location and length of the twist axis must be determined as follows. (Refer to Figure 26).

a. Starting at the lifted corner, visually run a line-of-sight along the lifted edge of the PWB to the point where the edge meets the granite plate surface. Mark this point for reference.

b. Return to the lifted corner and visually run a line-of-sight along the other lifted edge (making the 90 degree angle to the edge of item a in this list) and mark the reference point where the edge contacts the surface.

c. The twist axis is the straight line connecting the two reference points from items a and b. The length of this line (from PWB edge to PWB edge) is used for computing the twist factor.

d. The twist factor is determined by dividing the diameter of the pin gauge associated with the maximum deviation from the surface plate by the actual length of the twist axis from item c. The resulting factor in units of inch-per-inch (mm-per-mm) must be compared to the allowable values specified in DEC STD 176-0, subhead 3.4, Table 3 for all nonsurface mount products or DEC STD 176-4 subhead 3.2, Table 2 for all surface mount products.

C.6.3 BOW AND TWIST

Generally, many PWBs will exhibit both bow and twist to certain degrees. The issue to be addressed in each specific case will be to characterize which type of deviation from flatness will yield the maximum deviation between the PWB and the surface plate. The appropriate methodology to apply initially is to characterize the bow as in the text under subhead C.6.1 with the exception that measurements of bow along the length and width of the PWB have to be performed with at least two corners defining the length/width touching the surface plate. This must be done because the twist present in the PWB prevents all four corners from contacting the surface plate.

Once the maximum bow has been characterized and the bow factor has been computed, the maximum twist and twist factor must also be identified exactly as in the text under subhead C.6.2. The bow or twist factor for the PWB is the largest factor computed for either bow or twist and must be compared to the allowable values specified in DEC STD 176-0, subhead 3.4, Table 3 for all nonsurface mount products or DEC STD 176-4, Table 2 for all surface mount products.

APPENDIX D THERMAL STRESS TEST PROCEDURE

D.1 SCOPE

This procedure provides a standard method for testing and evaluating plated-through hole (PTH) copper plating, plated interconnections, and integrity of lamination. The test subjects specimens to a highly stressful thermal exposure simulating a single-assembly process thermal exposure or rework. The test can be performed on plated-through hole specimens any time after tin-lead reflow or solder coating is complete and meets the PWB thickness and quality requirements.

D.2 TEST SPECIMENS

This section describes the type and location for specimens.

D.2.1 SPECIMEN TYPE

Unless otherwise specified, test specimens can be sections removed from actual PWBs or special test coupons specifically characterized as being representative of the actual PWB.

D.2.2 SPECIMEN LOCATION

Unless otherwise specified, test specimens shall be taken from areas of the PWB where adverse thermal stress effects would be detrimental to the long-term reliability of the assembled module. Generally, these regions are not limited to but would include:

a. Areas of low current density (lower copper thickness)

b. Areas where aspect ratio is highest

c. Areas where B-stage resin fill is highest

d. Areas where inner-layer PTH interconnect is minimum

e. Areas where PTH density is highest (pin grid arrays, connectors, and so on)

If test specimens are special test coupons, the coupon design and location must be characterized to represent the conditions in the same manner as the PWB from which the coupon was obtained.

D.2.3 SPECIMEN DIMENSIONS/REMOVAL

Prior to the thermal stress test, it is recommended that the stress test specimens removed from the PWB (or coupon) initially be of larger dimensions, typically 2.0 inch $\times$ 2.0 inch (50.8 mm $\times$ 50.8 mm), than the final specimen size used for metallographic analysis. It is recommended that the specimens be carefully reduced to final dimensions following the thermal stress test as part of the metallographic specimen mounting procedure. The initial size of the specimen should be sufficient to contain the region of interest according

to the list under subhead D.2.2, plus an allowance for damage to the edges of the specimen created by the process of removing the specimen.

Specimens may be removed from the PWB by various mechanical techniques such as routing, punching, diamond sawing, or shearing. Each technique differs with respect to productivity and degree of edge damage. The initial size of the test specimen must make allowance for the degree of edge damage that the results of the stress test are not affected by the specimen removal process.

Unless otherwise specified, the final dimensions of the test specimen must be consistent with the size of the region of interest per the list under subhead D.2.2 and the size of the mounting ring or fixture used to prepare the sample for metallographic analysis following the test.

Regardless of whether the specimen dimensions are different prior to or after the stress test, the process of removing the specimens and preparing the metallographic samples for analysis must have no measurable effect on the results of the stress test.

D.2.4 QUANTITY OF TEST SPECIMENS

The actual quantity of test specimens (or coupons) per PWB must be sufficient to provide a statistically representative sample of the PWB for the purposes of the test. In addition, the sampling frequency must be sufficient to provide a statistically representative sample of the manufacturing process (for process control testing), manufactured lot (for lot acceptance), or qualification lot (for qualification acceptance).

The specific quantity and sampling frequency will not be specified here but are to be determined by agreement between the PWB supplier and all groups affected (product engineering, module assembly). The agreed upon specimen quantity and sampling frequency are to be included in local PWB supplier procedures where the stress test is required.

D.3 APPARATUS

This section describes the apparatus used to test for thermal stress.

D.3.1 BAKE OVEN

The oven chamber must be of the circulating air type with sufficient capability of maintaining 135°C (275°F) minimum to 149°C (300°F) maximum.

D.3.2 SOLDER POT

The solder pot must be of sufficient size to contain at least two pounds of solder and test specimens. The pot must have sufficient thermostatic control to maintain solder temperature at 287 ± 6°C (550 ± 10°F) as measured 3/4 ± 1/4 inch (19.05 ± 6.35 mm) below solder surface for period of 10 seconds +1/-0 seconds.

D.3.3 SOLDER

Minimum 2 pounds of allowed composition range Sn60, Sn62, or Sn63 per Federal Specification QQ-S-571 *Solder, Tin Alloy: Tin-Lead; and Lead Alloy.*

D.3.4 TEMPERATURE INDICATOR

A thermocouple or other device capable of accurately measuring solder temperature 3/4 ± 1/4 inch (19.0 ± 6.35 mm) below solder surface is required.

D.3.5 FLUX

The flux used must be type RMA per *MIL-F-14256 Flux, Soldering, Liquid*.

D.4 PROCEDURE

This section describes the procedure used to test thermal stress.

D.4.1 OVEN CONDITIONING

Specimens shall be conditioned by drying in an oven at 135°C to 149°C (275°F to 300°F) for a minimum of six hours to remove moisture and relieve stress. More complex specimens may require longer conditioning time. Following oven conditioning, samples shall be cooled to room temperature in a desiccator.

D.4.2 FLUXING

Remove specimens from the desiccator and completely flux coat the surfaces and plated-through holes to insure solder wetting and hole fill during and after the test.

D.4.3 SOLDER FLOAT

Remove any dross from solder surface and lay the specimen on the solder maintained at 287 ± 6°C (550 ± 10°F) for a period of 10 seconds +1/-0 seconds. Solder temperature shall be measured at a depth of 3/4 ± 1/4 inch (19.05 ± 6.35 mm) below the solder surface. Specimens should not be held against or pushed into the solder during the test.

D.4.4 SPECIMEN COOL DOWN

Following solder float, the specimens shall be carefully removed from the solder and placed on a ceramic plate to cool to room temperature. It is important that the specimens not be excessively shocked mechanically while the solder in the plated-through holes is still molten. In addition, the rate of cool down of specimens must not be accelerated by any means other than simple cool down to typical laboratory standard temperature and pressure environmental conditions (25°C/1 atmosphere).

NOTE

When more than one thermal stress test is performed, steps mentioned in D.4.2 through D.4.4 above shall be repeated in sequence.

D.4.5 SPECIMEN PREPARATION FOR METALLOGRAPHIC ANALYSIS

Once samples are at room temperature, specimens can be reduced to final dimensions for microsectioning. This must be accomplished carefully using low distortion and damaging methods (such as metallographic diamond saw or metallographic sanding equipment of 180 grit or finer) to reduce the sample size to approximately 0.050 inch (1.27 mm) of final polish depth.

D.4.6 MICROSECTION PREPARATION

Prepare microsection as defined in IPC-TM-650; test method 2.1.1.

D.4.7 MICROSECTION ANALYSIS

Unless specified otherwise, examine the integrity of foil, plating, plated interconnections, and lamination according to the requirements under DEC STD 176-0 subheads 5.2.2 and 5.2.3.

APPENDIX E METRIC HOLE SIZE SELECTIONS CORRESPONDING TO DIGITAL STANDARD U.S. CUSTOMARY REQUIREMENTS

These practical metric hole size selections correspond to standard U.S customary requirements and consider both U.S. customary and metric drill sizes.

Table 15: Metric Hole Size Selections

Inches	Tolerance	Millimeters	Tolerance
		VIAS	
.01	+0.003 / -0.01	0.25	+0.08 / -0.25
.015	+0.003 / -0.015	0.40	+0.08 / -0.40
.02	+0.003 / -0.02	0.50	+0.08 / -0.50
		COMPONENTS	
0.020	+0.004 / -0.002	0.50	+0.10 / -0.05
0.028	+0.003 / -0.002	0.70	+0.09 / -0.05
0.030	±0.003	0.75	±0.08
0.032	±0.003	0.80	+0.09 / -0.06
0.034	±0.003	0.85	+0.09 / -0.06
0.035	±0.003	0.90	+0.06 / -0.09
0.038	+0.004 / -0.003	0.95	+0.12 / -0.06
0.041	+0.002 / -0.003	1.05	+0.04 / -0.08 (press fit)
0.042	+0.005 / -0.003	1.10	+0.09 / -0.11
0.046	±0.004	1.20	+0.07 / -0.13
0.055	±0.004	1.40	±0.10
0.059	±0.004	1.50	±0.10
0.062	±0.004	1.60	±0.10
0.067	±0.005	1.70	±0.13
0.076	±0.005	1.95	±0.13
0.082	±0.005	2.10	±0.13
0.101	±0.005	2.55	±0.13
0.125	±0.010	3.20	±0.25

Table 15 (Cont.): Metric Hole Size Selections

Inches	Tolerance	Millimeters	Tolerance
		NOT PLATED THRU	
0.125	±0.005	3.20	+0.10 / -0.15
0.133	±0.005	3.40	+0.10 / -0.15
0.157	±0.005	4.00	+0.12 / -0.14
0.157	±0.002	4.00	+0.04 / -0.06 (module alignment)
0.187	±0.005	4.75	±0.13
0.250	+0/-0.003	6.35	+0/-0.08

APPENDIX F PRINTED-WIRING BOARD CONFIGURATIONS

F.1 CONFIGURATIONS

Table 16 shows obsolete PWB configurations that applied to DEC STD 176-0 revisions prior to Revision M. It is included here for historic reference only.

Table 16: Printed-Wiring Board Configuration

		Layer Code									
		A	B	C	D	E	F	G	H	J	K
Technology line/ space	line/ space code	Single–Sided No PTH	Double–Sided No PTH	Double–Sided PTH	4 ML 2 sig 2 PG	6 MSL 2 sig 2 PG 2 pad	6 MSL 4 sig 2 PG	8 MSL 4 sig 2 PG 2 pad	8 MSL 6 sig 2 PG	10 MSL 4 sig 4 PG 2 pad	10 MSL 6 sig 4 PG
25/25	A	AA	AB	AC							
20/20	B	BA	BB	BC	BD						
15/15	C	CA	CB	CC	CD						
12/13	D	DA	DB	DC	DD			DG			
8/8	E	EA	EB	EC	ED						
6/10	F					FE		FG		FJ	FK
5/5	G									GJ	GK

APPENDIX G REFERENCED DOCUMENTS

G.1 Digital Documents, EL-Class

Document Number	Document Title
76-65158-00	*Hollis TDC-16A Wave Soldering System: Process Control*
EL-00016-00	*DEC STD 016-0 Printed-Wiring Board and Module Manufacturing Terminology*
EL-00176-01	*DEC STD 176-1 Printed-Wiring Board Repair Criteria*
EL-00176-02	*DEC STD 176-2 Printed-Wiring Board Product Safety Criteria*
EL-00176-04	*DEC STD 176-4 Surface Mount Printed-Wiring Board Acceptance Criteria*
EL-00176-06	*DEC STD 176-6 Single-Sided/Double-Sided Nonplated Through (SS/DS) Printed-Wiring Board Acceptance Criteria*
EL-ENPCB-01	*PC Board Engineering Handbook - Standard Circuit and Finger Details*
EL-ENPCB-02	*PC Board Engineering Handbook—Layer Construction Drawings*
EL-MF299-00	*Printed-Circuit Boards/Modules: Cleaning Process Contamination*
EL-MF543-00	*Procedure for Soldermask Evaluation*
EL-MF601-00	*Test Method for Soldermask Cure*
EL-SM176-00	*Printed-Wiring Board Manual*

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

G.2 Documents External to Digital

Document Number	Document Title
AMP 109-146	*Porosity, Nitric Acid, Vapor, AMP Incorporated Test Specification, No. 109-146, Rev o*

G.3 Digital Drawings

Document Number	Document Title
C-MD-ELEN627-00-DBU	*Layer Construction, Board, Single-Sided, Non-PTH*
C-MD-ELEN628-00-DBU	*Double-Sided, Non-PTH*
C-MD-ELEN629-00-0	*Layer Construction, Board, Double-Sided, PTH*
C-MD-ELEN630-00-DBU	*Layer Construction, Board, 4-Layer*
D-MD-ELEN631-00-DBU	*Standard Layer Construction Detail, 6-Layer Board*
D-MD-ELEN632-00-DBU	*Standard Layer Construction Detail, 8-Layer Board*
D-MD-ELEN633-00-DBU	*Generic Layer Construction VAXBI Module Detail—10 Layer Board*
D-MD-ELEN635-00-DBU	*XMI Module Detail—10-Layer Module Construction*

These drawings are contained in A-MN-ELENPCB-02-0 *PC Board Engineering Handbook—Layer Construction*. This handbook can be obtained from:

Standards and Methods Control
$ VTX SMC, JOKUR::SMC, DTN: 234-4423, or NRO5/I2.

Please provide your name, mailstop, cost center, badge number, and node address when ordering.

G.4 Digital Purchase Specifications

Document Number	Document Title
A-PS-1400000-GS	*Basic Specification for Printed-Wiring Board Materials*
A-PS-1400001-GS	*Glass Epoxy Panels (No Copper)*
A-PS-1400002-GS	*Micarta Panels (Blue and Black)*
A-PS-1400008-GS	*Copper-Clad Thin Laminates (Raw Stock 0.031 Inches Thick or Less)*
A-PS-1400009-GS	*Preimpregnated Glass Cloth (B-Staged)*
A-PS-1400011-GS	*Copper-Clad Thick Laminate (Raw Stock > 0.031 Inch Thick)*
A-PS-1400015-GS	*Copper Foil for PWBs—Sheets and Rolls*
A-PS-1400016-GS	*Mass Molded Laminates*
A-PS-1400017-GS	*Preimpregnated Glass Cloth for Multisignal Lay PWBs*
A-PS-1400018-GS	*Copper-Clad Thin Laminates for Multisignal Layer PWBs*
A-PS-1400023-GS	*Polyimide Copper-Clad Laminates for ML PWBs*
A-PS-1400024-GS	*Polyimide Preimpregnated Glass Cloth (B Stage) for ML PWBs*
A-PS-1400025-GS	*Copper Clad Laminates Utilizing Planar Resistor Foils*
A-PS-1400026-GS	*CEM-3 Copper-Clad Thick Laminates (Raw Stock >0.031 Inch)*
A-PS-1400027-GS	*Laminates, Copper-Clad for Multilayer PWBs Utilizing Bismalemide-triazine*
A-PS-1400028-GS	*Bismalemide-triazine Preimpregnated Glass Cloth (B-Stage) for Multilayer PWBs*
A-PS-1400029-GS	*Soldermask—Photoimageable Liquid or Screened Liquid*
A-PS-1400030-GS	*Soldermask - Photosensitive Dry Film*
A-PS-1400031-GS	*Copper Chelating Material (Coating) All Copper*

Copies of these Purchase Specifications can be obtained from your local microfiche/microfilm library or the SPOC system.

For hard copy distribution, contact:

Specification Control Systems
NR05/M2, DTN: 234-5077

Non-Digital Equipment Corporation PWB suppliers may obtain copies of these documents from the appropriate Digital purchasing agent.

G.5 Federal and Military Publications

Document Number	Document Title
A-A-113 (Formerly L-T-90)	*Tape, Pressure-Sensitive Adhesive (Cellophane and Cellulose Acetate)*
QQ-N-290	*Nickel Plating, Electrodeposited*
QQ-S-571	*Solder, Tin Alloy: Tin-Lead; and Lead Alloy*
MIL-C-14550	*Copper Plating, Electrodeposited*
MIL-F-14256	*Flux, Soldering, Liquid*
MIL-G-45204	*Gold Plating, Electrodeposited*
MIL-P-81728	*Plating, Tin-lead, Electrodeposited*

Copies of these federal and military publications may be obtained free of charge from:

The Naval Publications and Forms Center
5801 Tabor Ave., Philadelphia, PA 19120
Telephone (215) 697-3321

G.6 IPC (Institute of Printed Circuits) Publications

Document Number	Document Title
IPC-CF-150	Copper Foil For Printed Wiring Applications
IPC-T-150	Terms and Definitions of Interconnecting and Packaging Electronic Circuits
IPS-S-804	*Solderability Test Methods for Printed Wiring Boards*
IPC-SM-840A	*Qualification and Performance of Permanent Polymer Coating (Soldermask) for Printed Boards*
IPC-TM-650	*Test Methods Manual*
	Porosity of Metallic Coatings on Copper-Base Alloys, and Nickel (Nitric acid vapor test), Number 2.3.24.2

Copies of these IPC publications may be purchased from:

The Institute for Interconnecting and Packaging Electronic Circuits
7380 North Lincoln Ave., Lincolnwood IL 60646
Telephone (708) 677-2850

G.7 Other Publications

Document Number	Document Title
ASTM E53-48	*Standard Method for Chemical Analysis of Copper (Electrolytic Determination)*
UL-94	*Test for Flammability*

Copies of the ASTM publication may be purchased from:

The American Society for Testing and Materials
1916 Race St., Philadelphia, PA 19103
Telephone (215) 299-5400

Copies of the UL publication may be purchased from:

Underwriters Laboratories, Publication Stock
333 Pfingsten Rd., Northbrook IL 60062
Telephone (312) 272-8800

APPENDIX H RELATED DOCUMENTS

H.1 Digital Purchase Specifications

Document Number	Document Title
A-PS-1400003-GS-0	*Copper Foil, Polyimide*
A-PS-1400006-GS-0	*Multilayer Purchase Specification*

Copies of these Purchase Specifications can be obtained from your local microfiche/microfilm library or the SPOC system.

For hard copy distribution, contact:

Specification Control Systems
NR05/M2, DTN: 234-5077

PWB suppliers external to Digital may obtain copies of these documents from the appropriate Digital purchasing agent.

H.2 Federal and Military Publications

Document Number	Document Title
MIL-F-14256	*Flux, Soldering, Liquid*

Copies of these federal and military publications may be obtained free of charge from:

The Naval Publications and Forms Center
5801 Tabor Ave., Philadelphia, PA 19120
Telephone (215) 697-3321

H.3 IPC (Institute of Printed Circuits) Publications

Document Number	Document Title
IPC-T-50	*Terms and Definitions for Interconnecting and Packaging Electronic Circuits*

Copies of these IPC publications may be purchased from:

The Institute for Interconnecting and Packaging Electronic Circuits
7380 North Lincoln Ave., Lincolnwood IL 60646
Telephone (708) 677-2850

H.4 Other Publications

Document Number	Document Title
ANSI Y14.5M-1982 (R 1988)	*Dimensioning and Tolerancing*
ASTM B735-84	*Standard Test Methods for Porosity In Gold Coatings On Metal Substrates By Gas Exposures*

The AMP Incorporated publication may be purchased from:

AMP Incorporated
939 East Park Drive
Harrisburg PA 17105

Copies of the ASTM publication may be purchased from:

The American Society for Testing and Materials
1916 Race St., Philadelphia, PA 19103
Telephone (215) 299-5400

INDEX

A

Abrasion resistance, 44
Additional ML and MSL Requirements
  Withstanding voltage (HIPOT), 51
Adhesion, 33, 35, 44, 55, 56
  Conformance, 44
Allowable repairs, 54
Annular rings
  Maximum allowable misregistration for non-MSL technologies, 26
Applicability, 63
Autothieving, 47

B

Backpanel boards, 47
Base material visual characteristics, 12
Beta backscatter instrument, 34
Bevel, 36
Blistering, 44
Bond strength (terminal pull strength), 33
Breaks, flaking, peeling and wrinkling, 37

C

Chips, cracks, fibers, and haloing—laminate, 12
Colors, 8
Composition and processing, 1
Conductor interconnection resistance, 51
Conductors and pads, 24
  Exposed, 45
  Widths, 24
Continuity, 51
Copper-clad laminates, 3
Crazing, measling, 12
Current capacity, 52

D

Delamination, 12, 14, 18
Dents, 37
Dielectric thickness, 10, 46
  Withstanding voltage, 56
Digital drawings, 1, 79
  Purchasing specifications, 3
Dimensions and tolerances, 8
Discolorations, 12, 37

E

Electroless copper, 4, 30
Electrolytic copper, 4, 30
  Gold, 4
  Nickel, 4
  Tin-lead, 4
Etch characteristics, 31
Exposed conductors and pads, 45

F

Fabrication materials, 2
Federal and Military Publications, 81, 83
Fingers, 10, 34
  Unused, 35
Flammability, 43, 55

G

General requirements, 1
Glass fiber protrusions, 17
Gold plating
  Critical contact area, 40
  Length, 40

H

Hex-board edge taper, 36
Holes, 14
  Extra, 14
  Missing, 14
  Plated-through holes (PTH), 15, 33
  Punched holes, 14
Holes and terminal areas, 33

I

Identification markings, 5
Inclusions, 37
Insulation Resistance, 52, 56
IPC (Institute of Printed Circuits) Publications, 81, 83
IPC-S-804, 33

IPC-SM-840, 4, 43
IPC-T-50, 63
IPC-TM-650, 2, 16, 24, 33, 35, 43, 44, 51, 52, 55, 56, 74

L

Laminates
  Copper-clad, 3

M

Maximum warpage, 11
Microsectioning and magnification, 2
ML and MSL boards
  Additional requirements, 51
MSL boards, 9, 46, 51

N

Nicks, 37
Nodules, 37
Nonplated hole diameters, 14

O

Outside configuration, 9
Overall configuration and construction, 1

P

Packaging, 54
Pad diameters, 25
Pattern accuracy
  Hole diameters, 15
  Nodules, 37
PC Board Engineering Handbook, 35
Pinholes, 37
Pits, 37
Placement defects, 45
Plated-hole diameters, 15
Plated-through holes (PTH), 15
Plating characteristics, 33
Plating materials, 4
  Thicknesses, 16
Porosity, 34
  Procedure, 34
Power and ground planes or thermal relief areas, 29
Prepreg, 3
Product Safety, 3
PTH diameters and tolerances, 10, 15
PWB Standards Committee, 1

Q

Quality assurance tests, 55

R

Referenced documents, 79
Related documents, 83

S

Scratches, 37
Slots, notches, and cutouts, 11
Solderability, 33
Soldermask, 4
Solder resistance, 44
Solvent and flux resistance, 43
Spacing, 24
  Finger-to-finger centerline, 35
Spacing/coverage requirements, 41
Straightness, parallelism, and squareness, 11
Suppliers, 1, 5, 80, 83
Surface conditions, 12
  Cure, 43
  Finish, 34
  Placement, 41
  Soldermask, 4
  Types, 41

T

Terminology, 1
Test Methods Manual, 2
Thermal impedance conductors (Legs), 24
Thermal stress
  Plated-through holes (PTH), 33
Thickness
  For fingerless boards, 9, 46
Tin-lead plating (fused), 33

V

Voids, 37, 45

W

Warpage, 11
Workmanship and cleanliness, 5

```
+---------------------------------------------------------------------+
|                          READER COMMENTS                            |
|                                                                     |
| Your  comments  and suggestions  will help  Standards and Methods   |
| Control improve their services and documents.                       |
+---------------------------------------------------------------------+
```

Did you request this document? _____ If so, did it arrive within a satisfactory period of time? _____ Please comment.

What are your impressions of this document? Consider format, organization, completeness, readability, and illustrations.

————————**FOLD ON THIS LINE**———————————————————— -

Did you find technical or clerical errors in this document? If so, please specify the page number(s) and the error(s).

Are the instructions for the update package clear? _____
Was an index available? _____ If not, is one needed? _____
Do you have other suggestions for improving this document?

The following information is optional:

Name _____ Mailstop _____

Department _____ Node _____

Send your comments to JOKUR::PROJECTS, or fold, staple, and send this page through interoffice mail to:

```
+------------------------------+
|       READERS' COMMENTS      |
| STANDARDS AND METHODS CONTROL |
|           NRO5/I2            |
+------------------------------+
```